

Fig. 1a

CENTRAL  
OFFICE  
INTERNET  
SERVICE  
PROVIDER

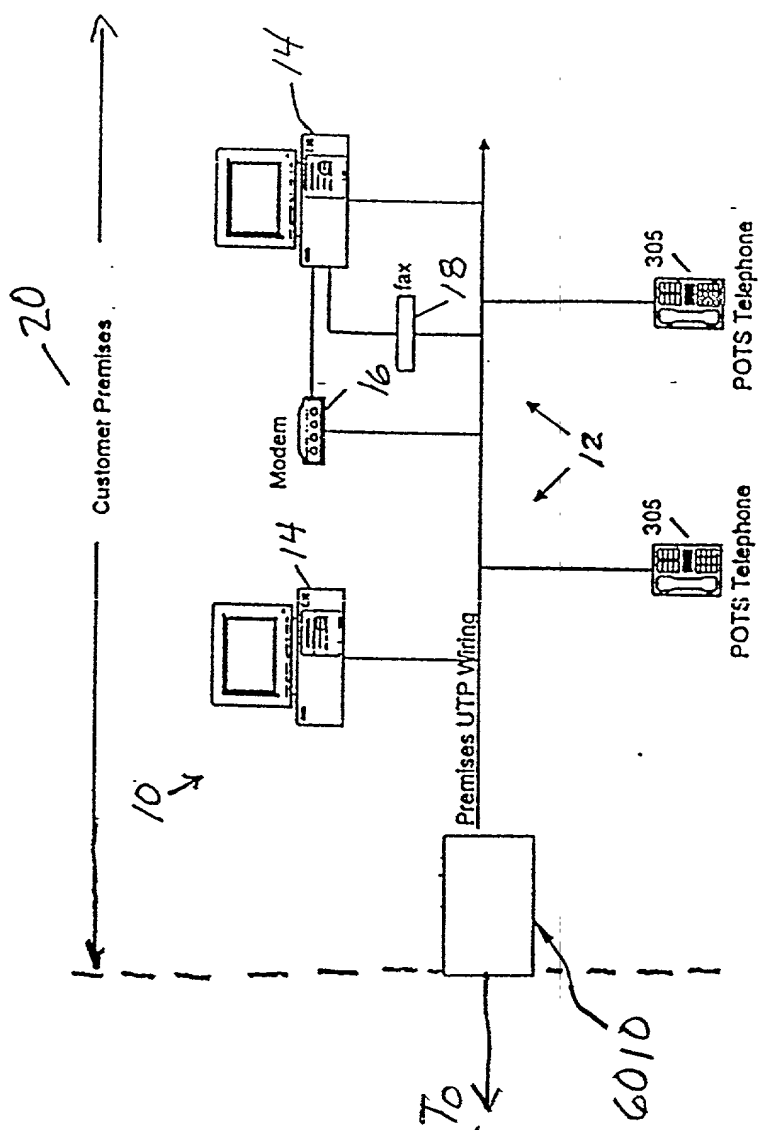
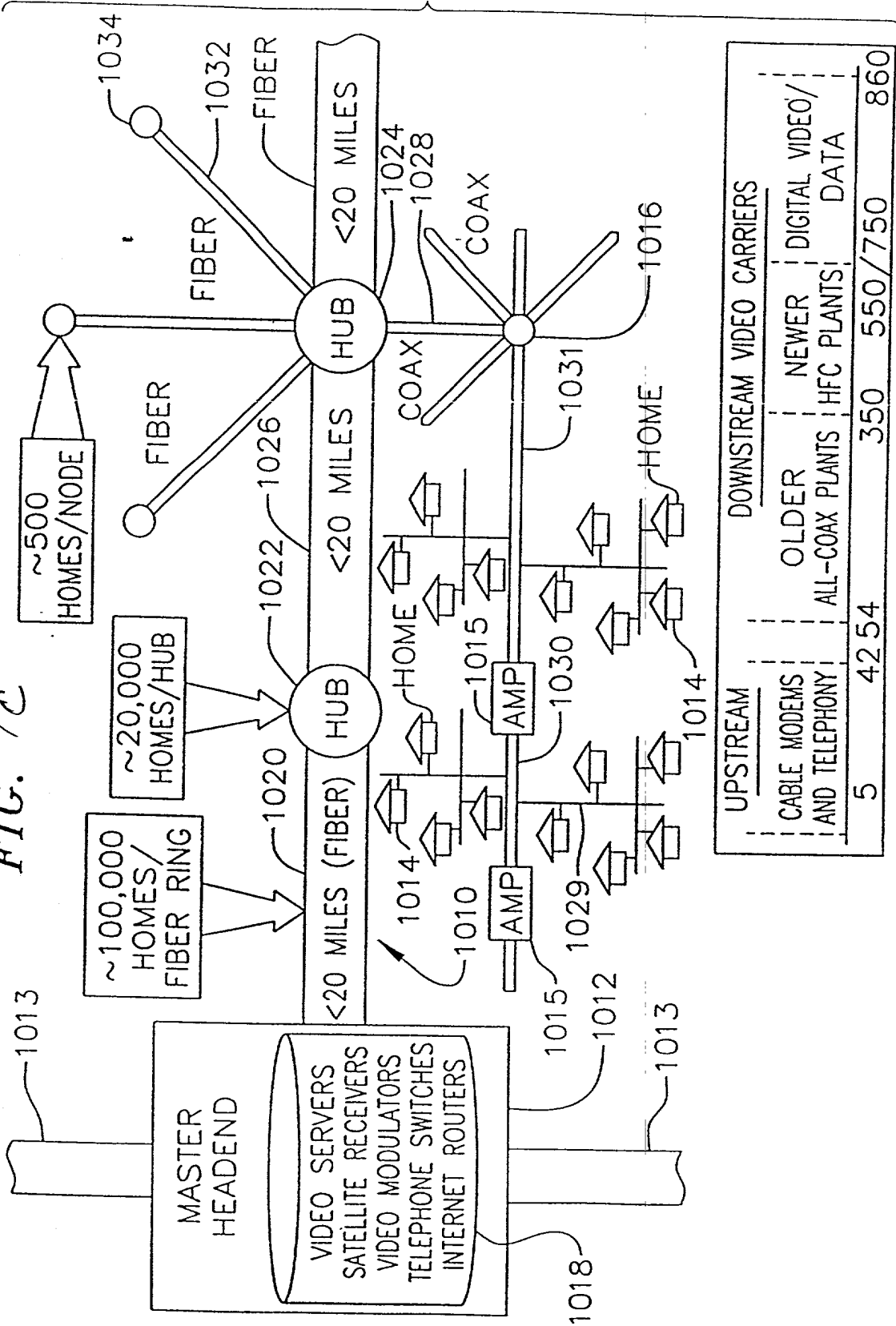


FIG. 1b

FIG. 1c



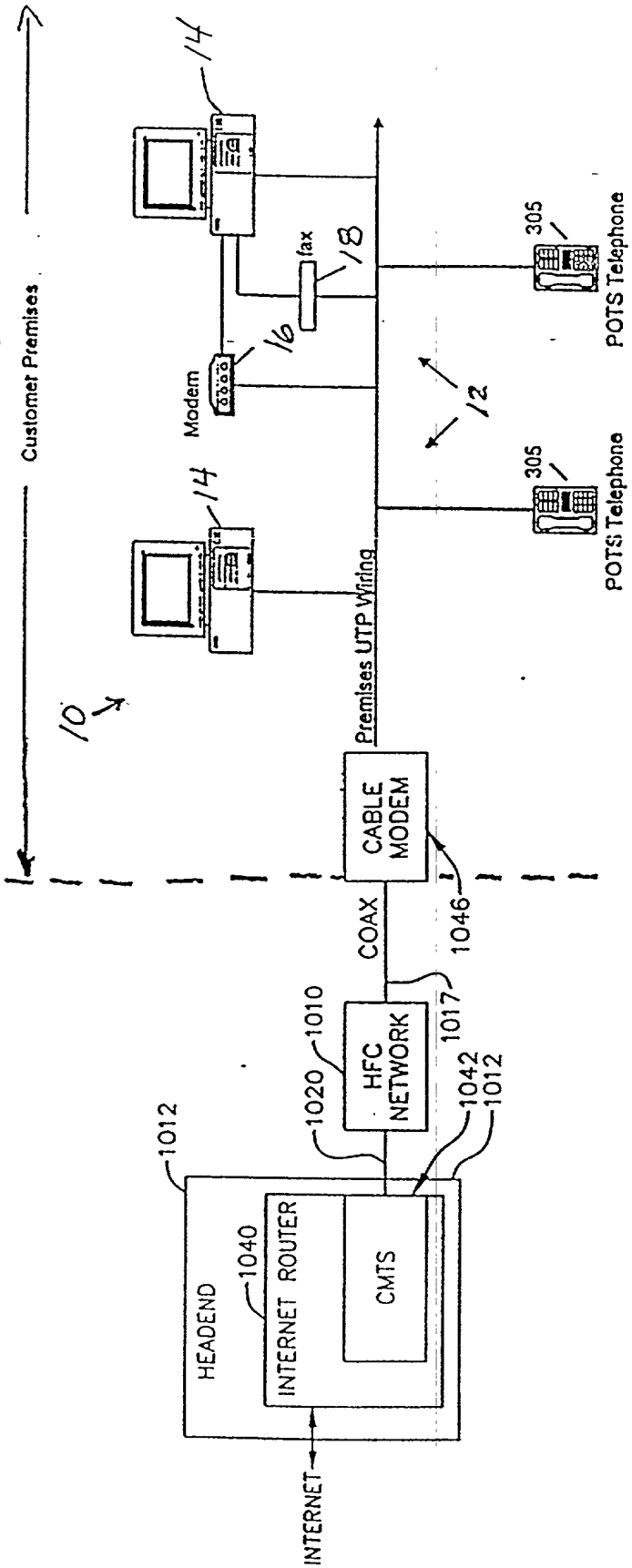


Fig 1d

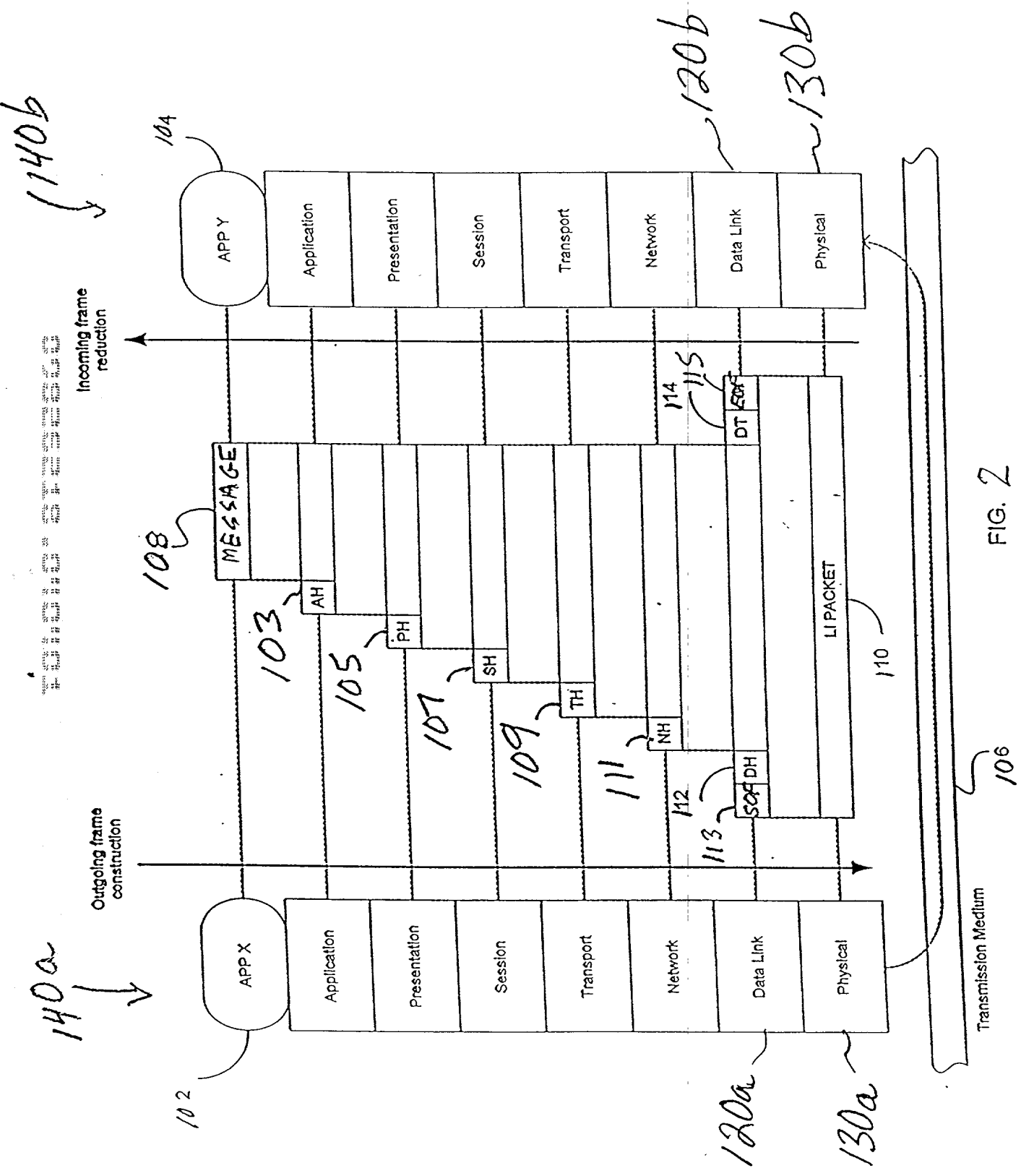


FIG. 2

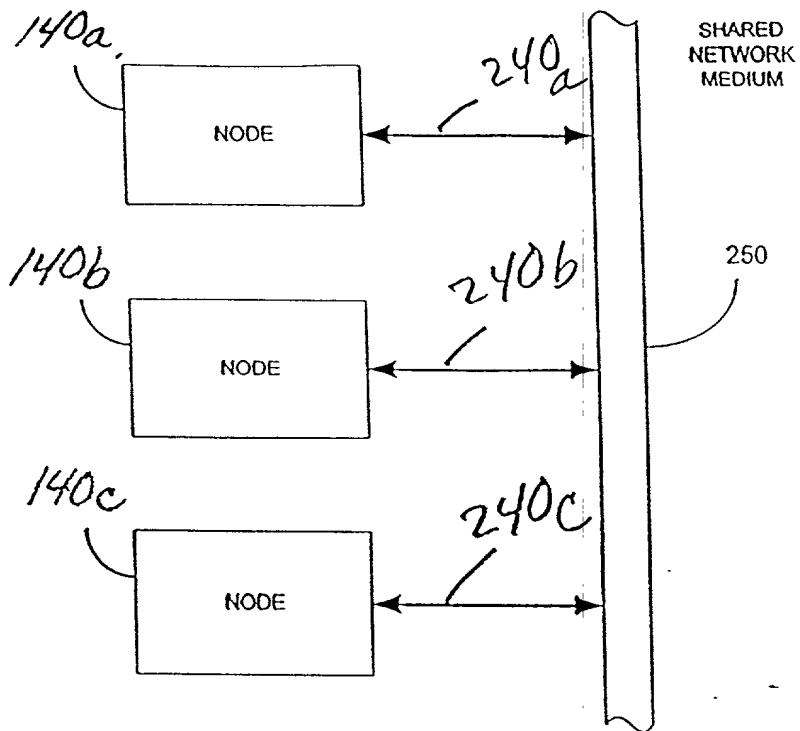


FIG. 3a

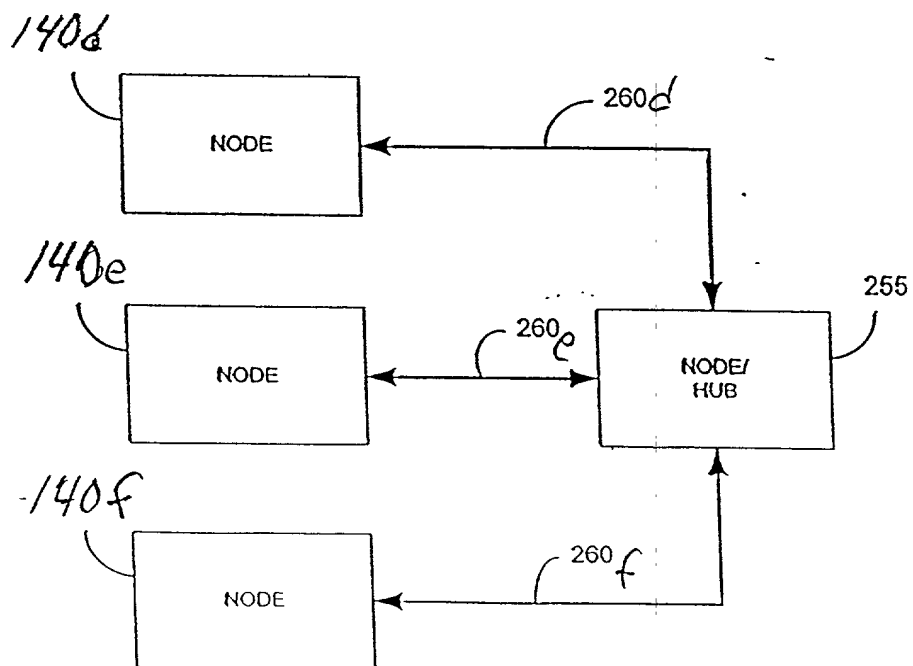


FIG. 3b

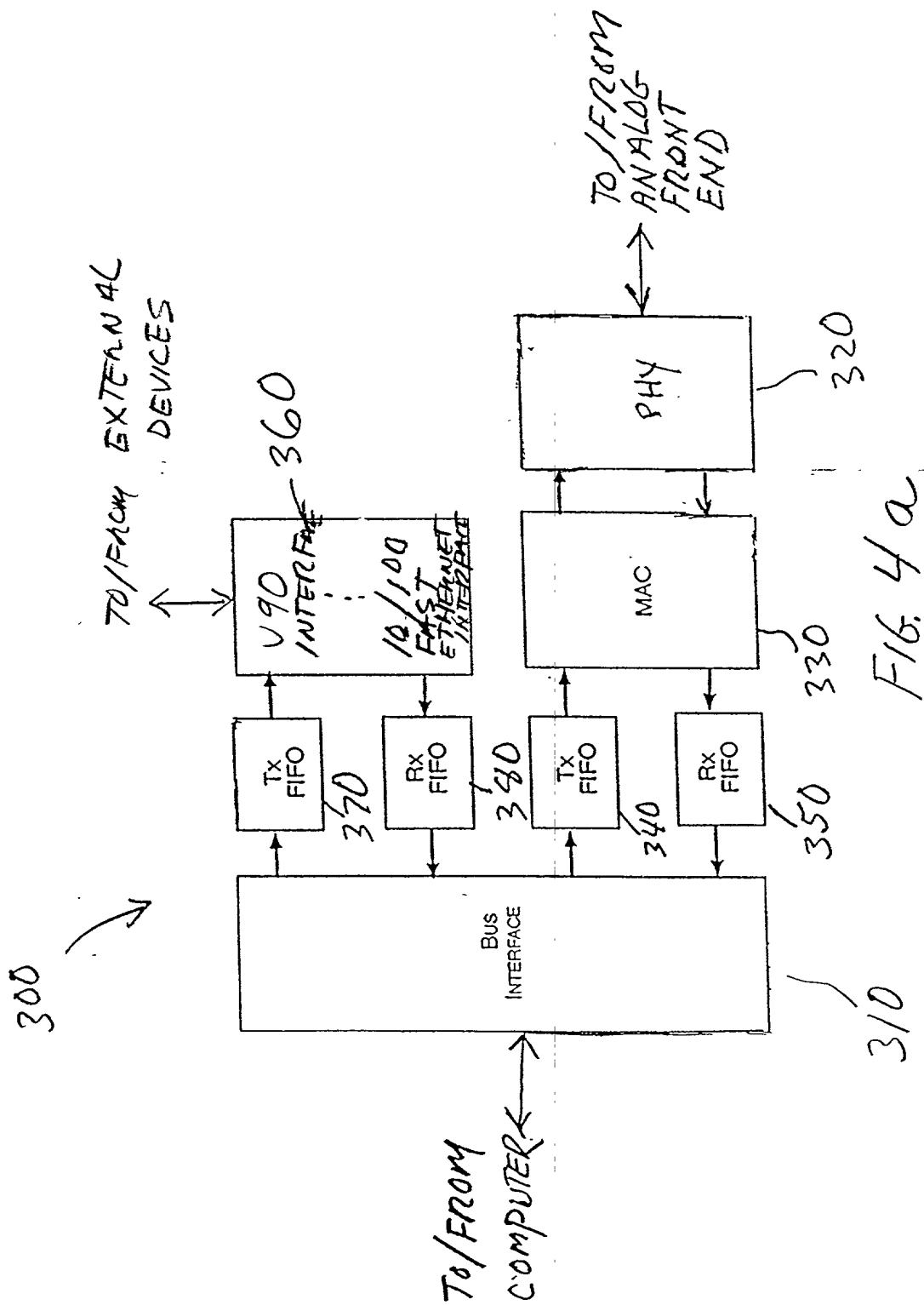


FIG. 4a

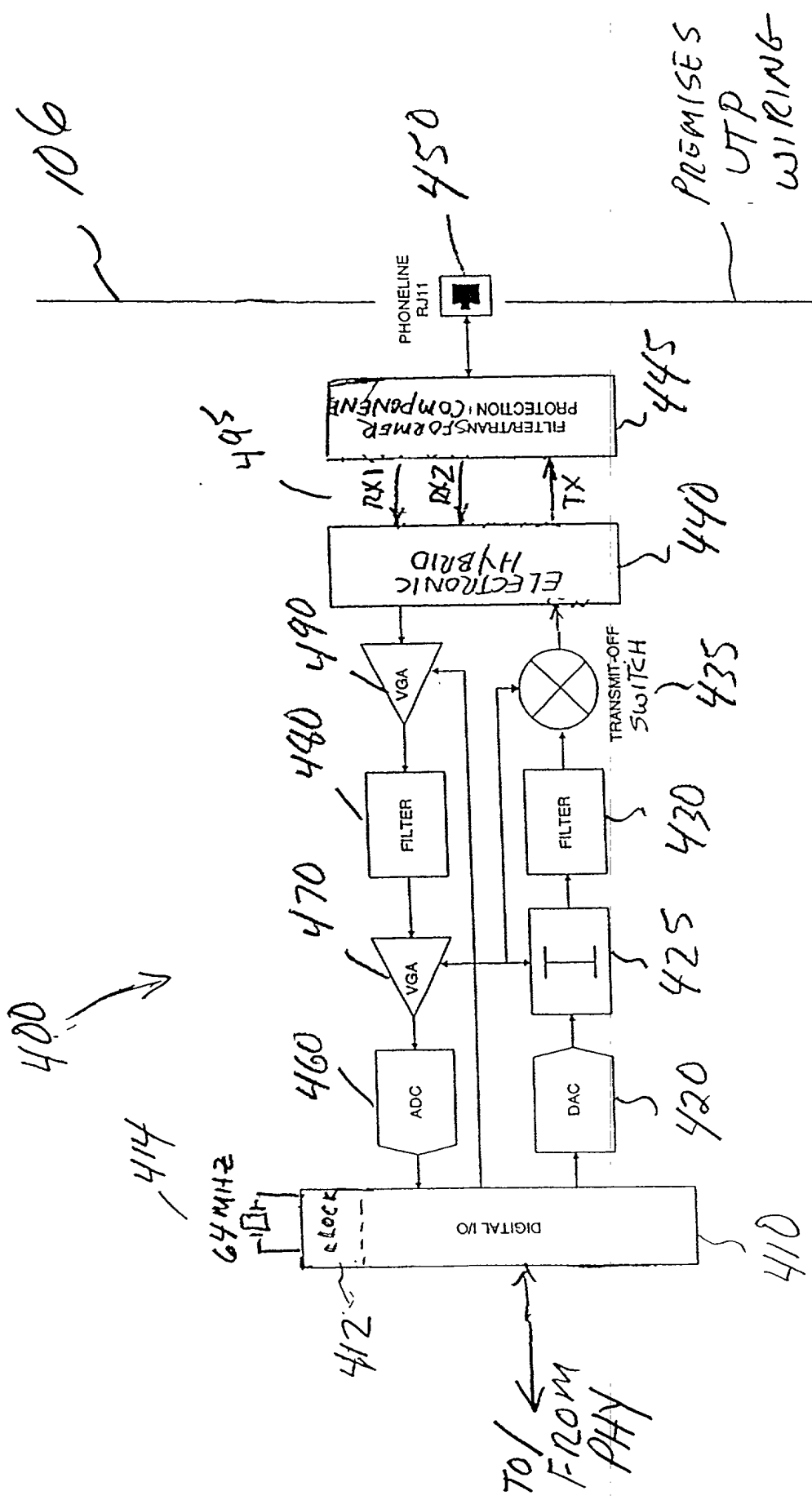


FIG-4b

500

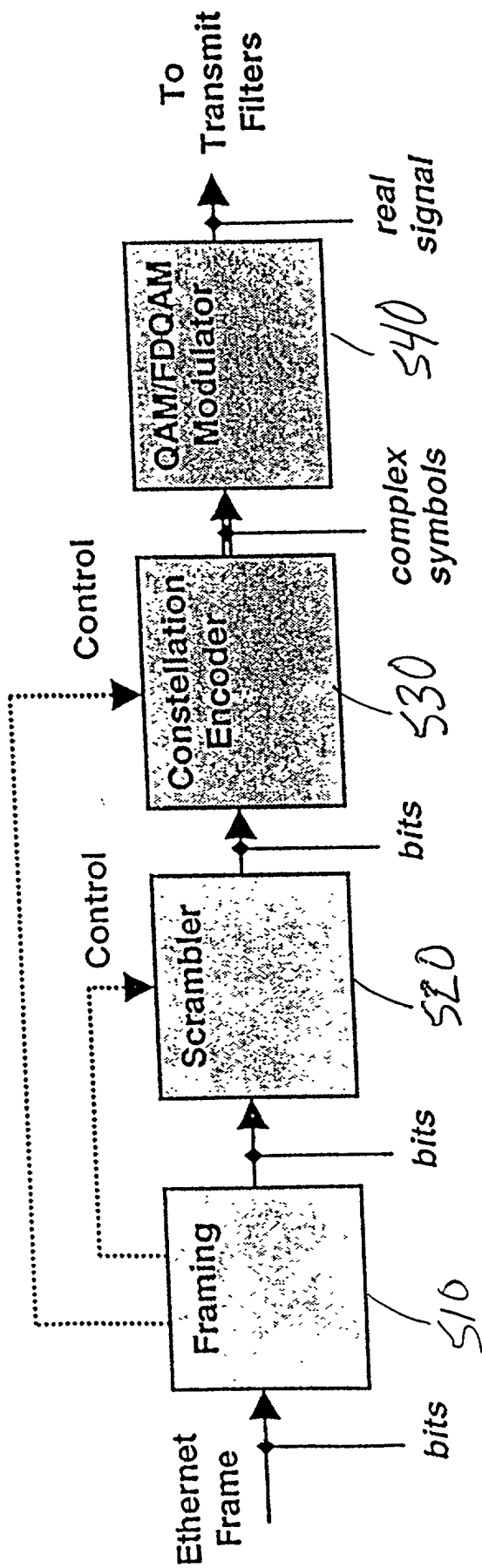


FIG 5.

632

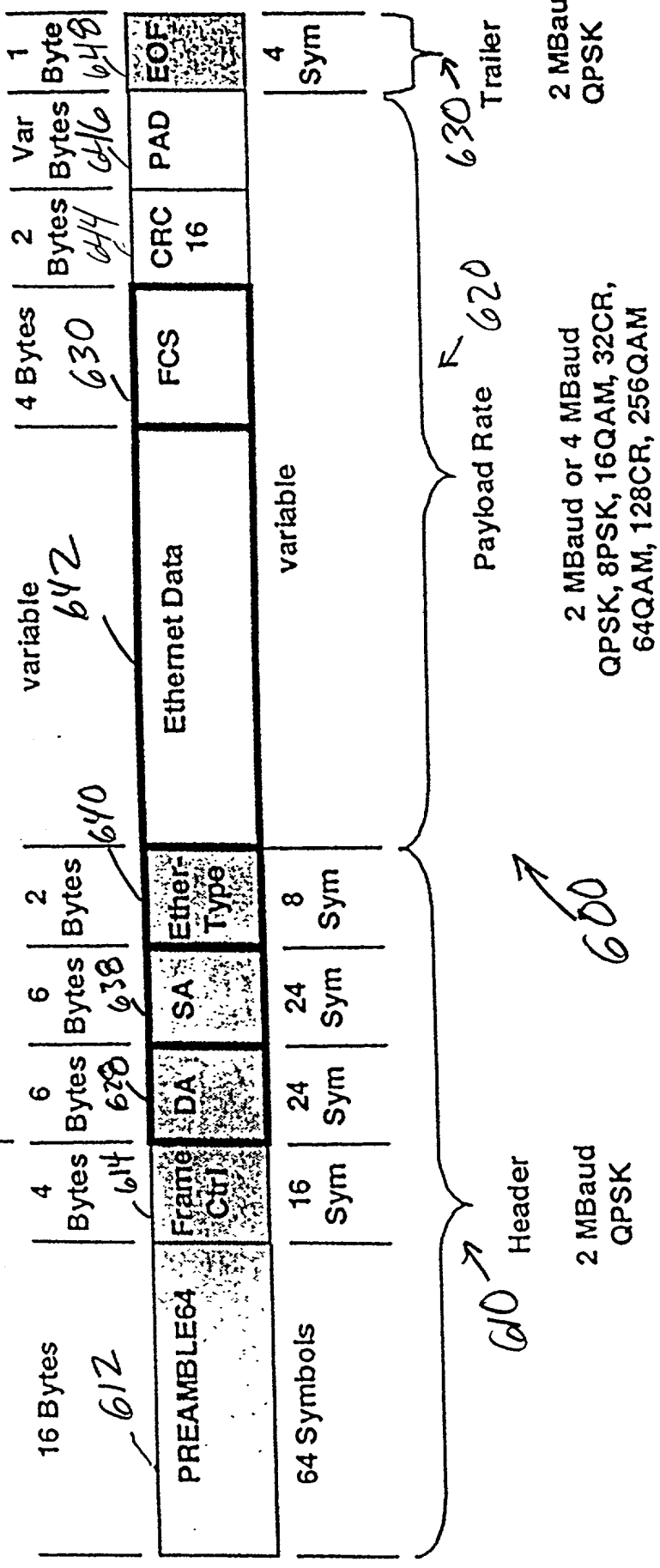
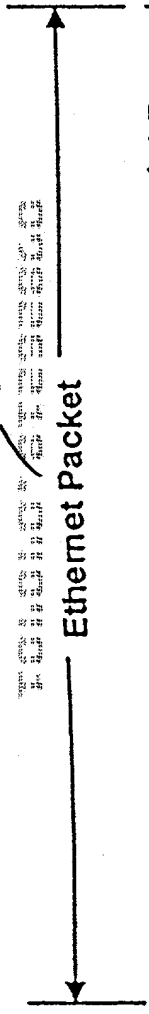
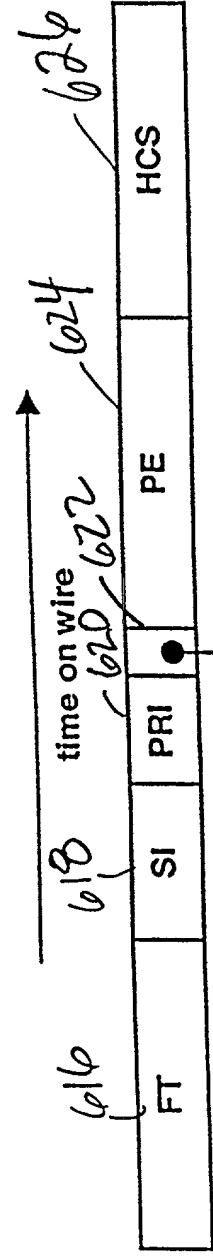


FIG. 6

□ = 4 Mbaud only



RSVD

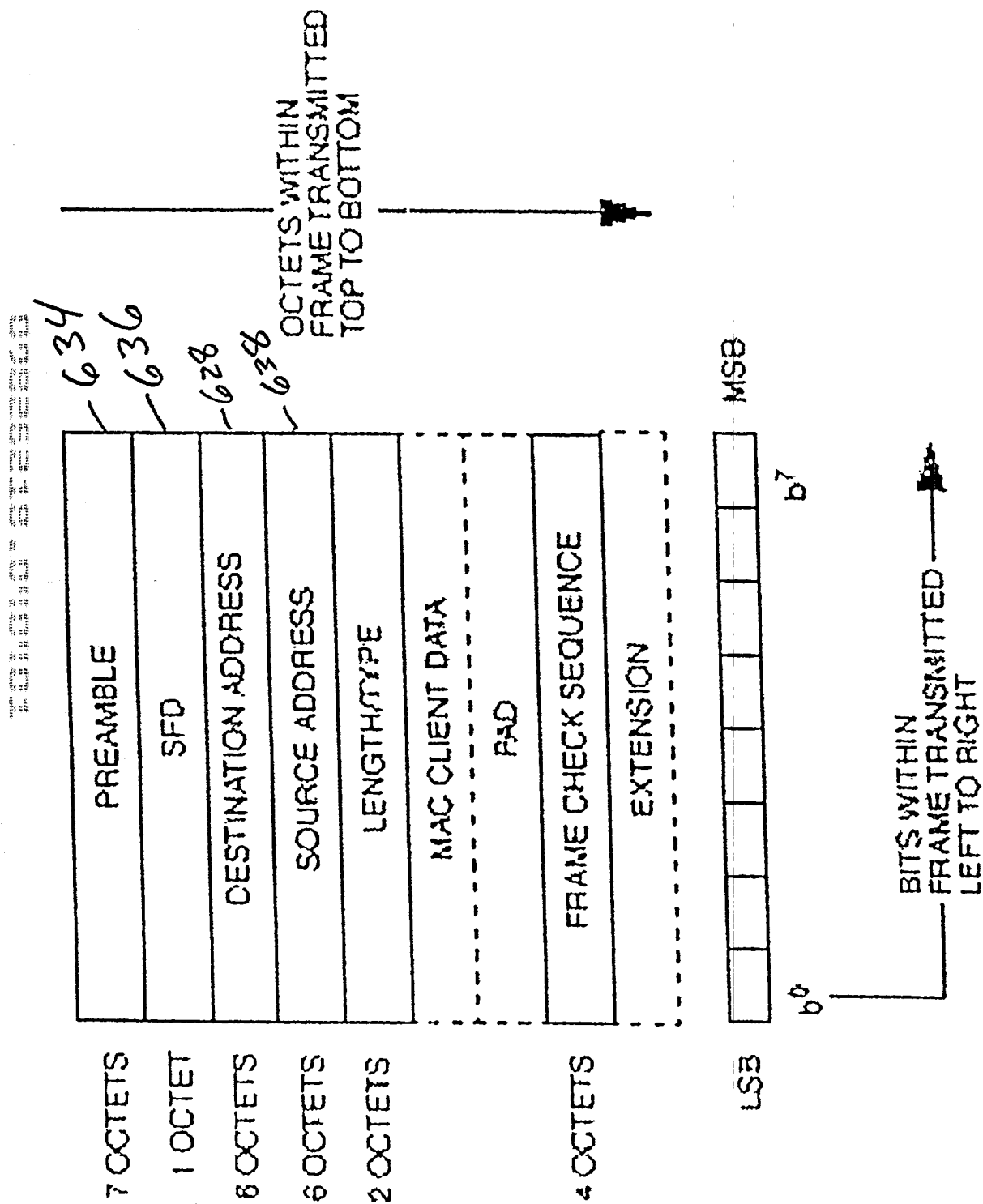
FIG. 8

614



Value	Interpretation
0	Reserved on transmit, discard frame on receive
1	Baud rate=2 MHz, 2 bits per Baud
2	Baud rate=2 MHz, 3 bits per Baud
3	Baud rate=2 MHz, 4 bits per Baud
4	Baud rate=2 MHz, 5 bits per Baud
5	Baud rate=2 MHz, 6 bits per Baud
6	Baud rate=2 MHz, 7 bits per Baud
7	Baud rate=2 MHz, 8 bits per Baud
8	Reserved on transmit, discard frame on receive
9	Baud rate=4 MHz, 2 bits per Baud
10	Baud rate=4 MHz, 3 bits per Baud
11	Baud rate=4 MHz, 4 bits per Baud
12	Baud rate=4 MHz, 5 bits per Baud
13	Baud rate=4 MHz, 6 bits per Baud
14	Baud rate=4 MHz, 7 bits per Baud
15	Baud rate=4 MHz, 8 bits per Baud
16-256	Reserved on transmit, discard frame on receive

FIG. 9



F16.10

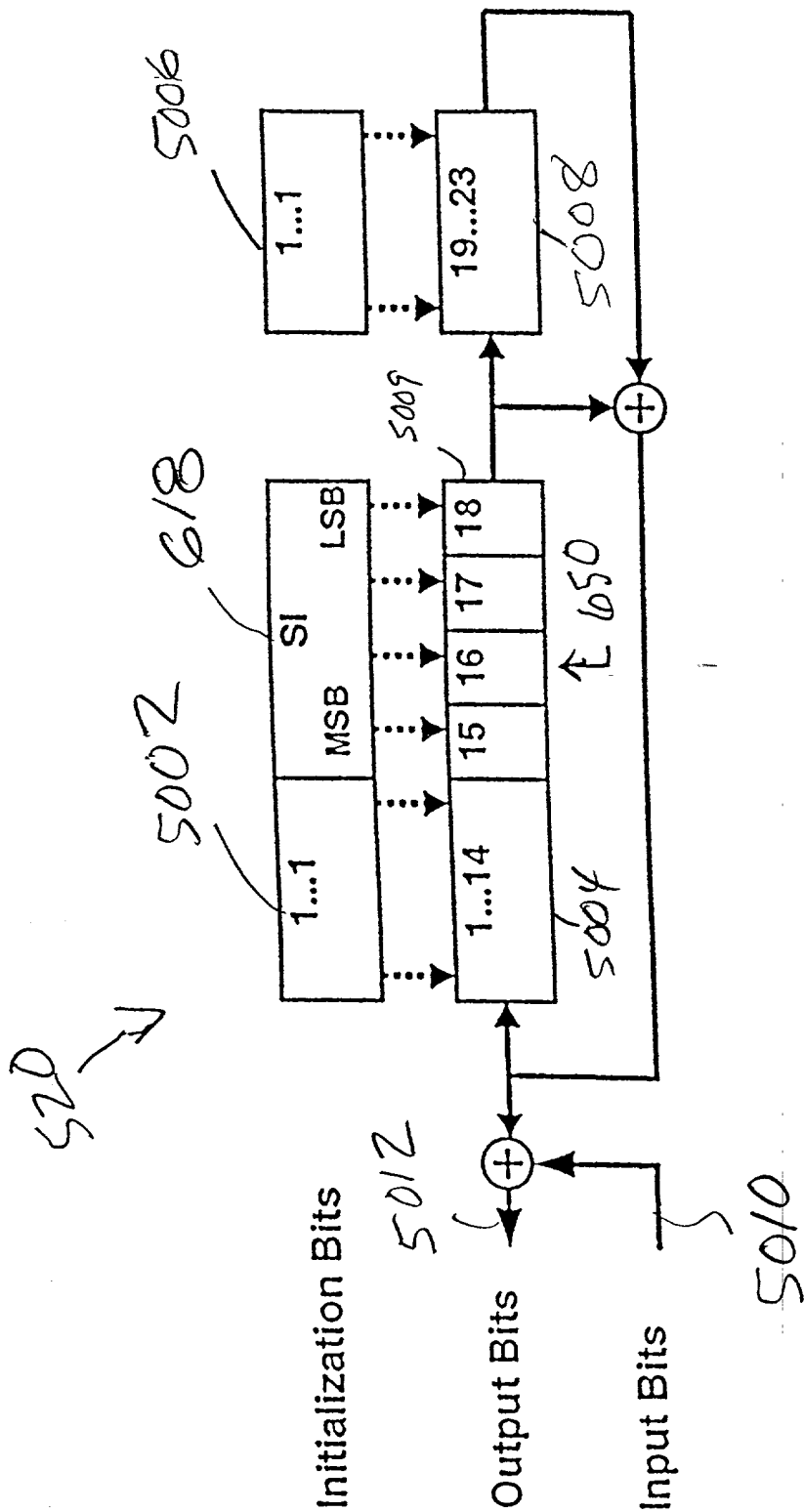


FIG. 11

Figure 12a, b, c, d show the bit patterns for 2, 3, 4, and 5 bits per baud. The bit patterns are shown in the tables below.

## 2 bits per Baud

01	00
11	10

FIG-12a →

## 4 bits per Baud

0111	0110	0010	0011
0101	0100	0000	0001
1101	1100	1000	1001
1111	1110	1010	1011

FIG →  
12c

## 3 bits per Baud

011	001
010	000
110	100
111	101

FIG-12b →

## 5 bits per Baud

01010	01110	00110	00010
01101	01100	00100	00111
01011	01001	00000	00001
01001	01000	00000	00011
11011	11001	10000	10011
11101	11100	10100	10111
11010	11110	10110	10010

FIG →  
12d

## 6 bits per Baud

011010	011011	011001	011000	001001	001011	001010
011110	011111	011101	011100	001101	001111	001110
010110	010111	010101	010100	000101	000111	000110
010010	010011	010001	010000	000001	000011	000010
110010	110011	110001	110000	100001	100011	100010
110110	110111	110101	110100	100101	100111	100110
111110	111111	111101	111100	101101	101111	101110
111010	111011	111001	111000	101001	101011	101010

7 bits PER BAUD

0101100	0101101	0111100	0111101	0001100	0001101	0001100	0001101
0100100	0100101	0110100	0110101	0010100	0010101	0000100	0000101
0110111	0110110	0110000	0110001	0010000	0010001	0010010	0010011
0111111	0111110	0111000	0111001	0011000	0011001	0011010	0011011
0101111	0101110	0101000	0101001	0001000	0001001	0001010	0001011
0100111	0100110	0100000	0100001	0000000	0000001	0000010	0000011
1100111	1100110	1100000	1100001	1000000	1000001	1000010	1000011
1101111	1101110	1101000	1101001	1001000	1001001	1001010	1001011
1110111	1110110	1110000	1110001	1010000	1010001	1010010	1010011
1111111	1111110	1111000	1111001	1011000	1011001	1011010	1011011
1101100	1101101	1110100	1110101	1001100	1001101	1001110	1001111
1101100	1101101	1111100	1111101	1011100	1011101	1011110	1011111

F/G. 12f →

8 bts per baud

F16. → 12g



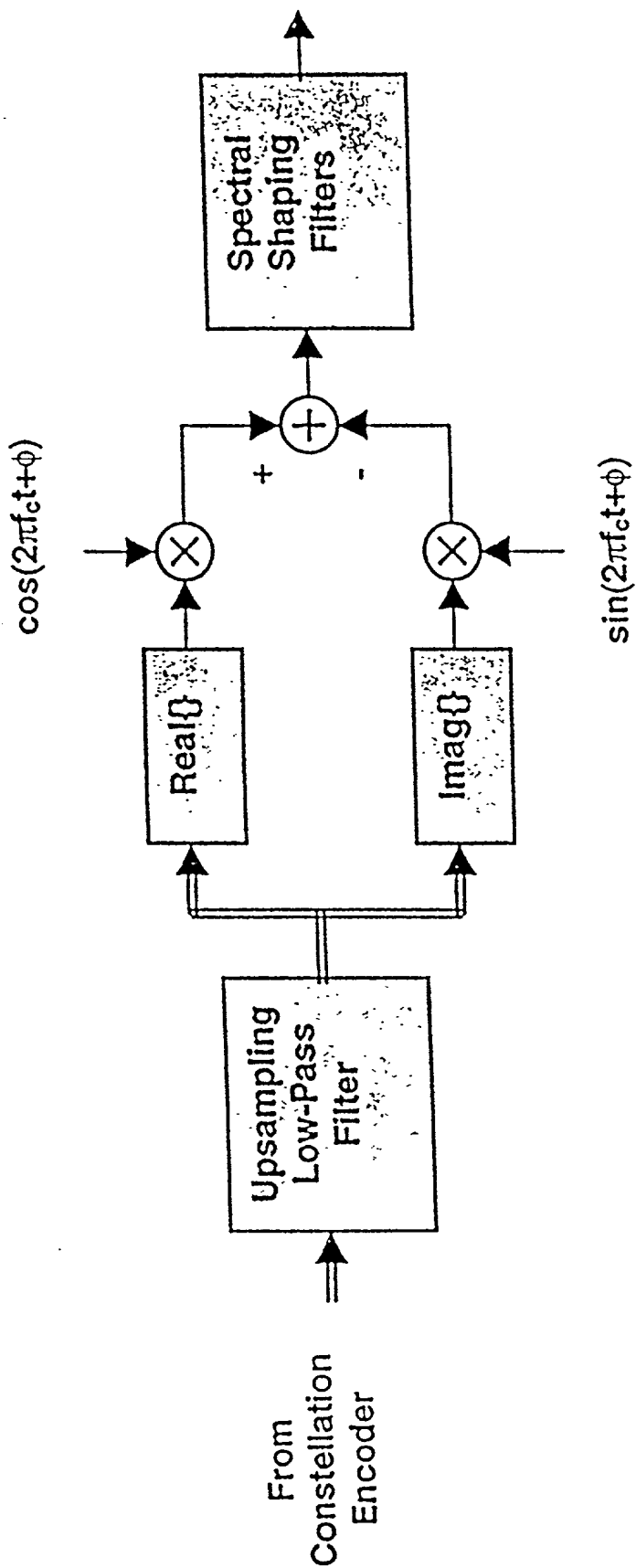


FIG. 15



FIG 16

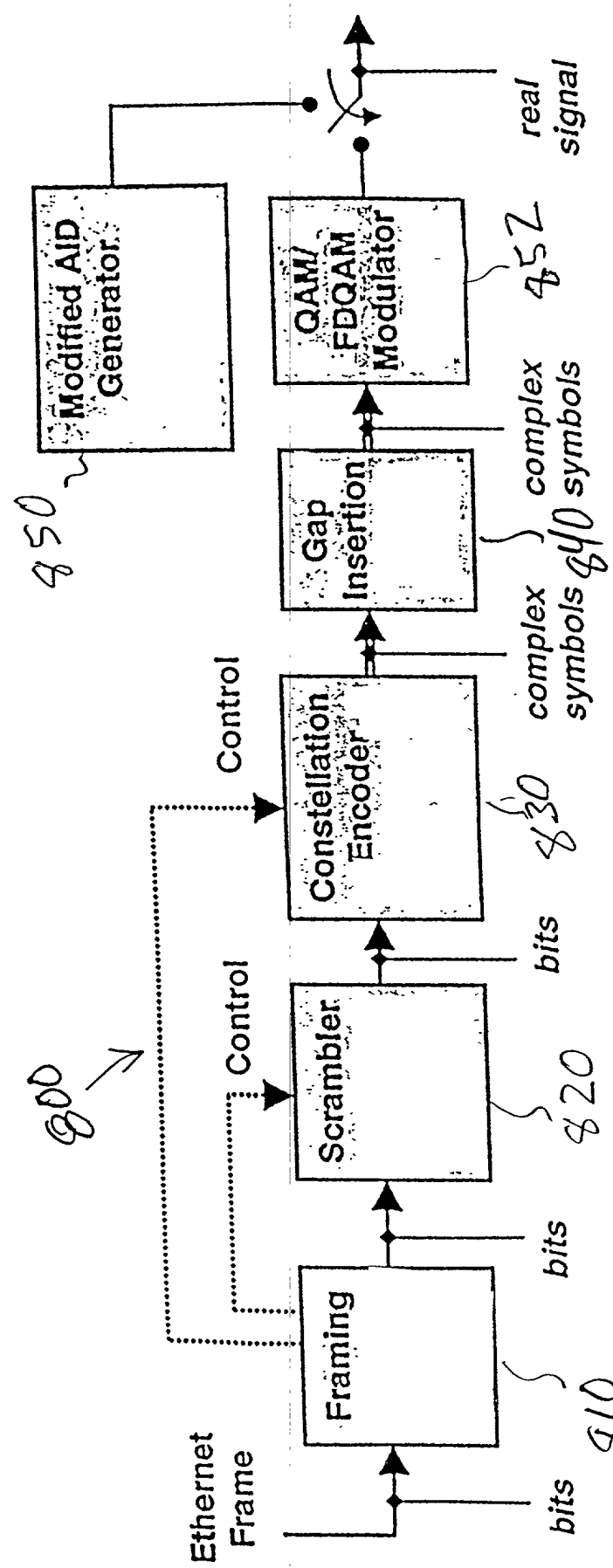


FIG 17



$M \bmod 2$	$P \bmod 2$	EOF/EOP sequence
0	0	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xfc</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 00</li> </ul>
0	1	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x03</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 11</li> </ul>
1	0	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x03</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 11</li> </ul>
1	1	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xfc</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 00</li> </ul>

FIG. 20

$M \bmod 2$	$P \bmod 4$	EOF/EOP sequence
0	0	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xfc</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 00</li> </ul>
0	1	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x56</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 10</li> </ul>
0	2	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x03</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 11</li> </ul>
0	3	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xa9</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 01</li> </ul>
1	0	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x03</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits, 11</li> </ul>
1	1	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xa9</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 01</li> </ul>
1	2	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0xfc</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 00</li> </ul>
1	3	<ul style="list-style-type: none"> <li>• 4 symbols, defined by the bits 0x56</li> <li>• 12 zero symbols</li> <li>• 1 symbol, defined by the bits 10</li> </ul>

Fig. 21

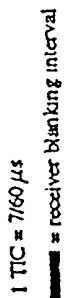


Fig. 22

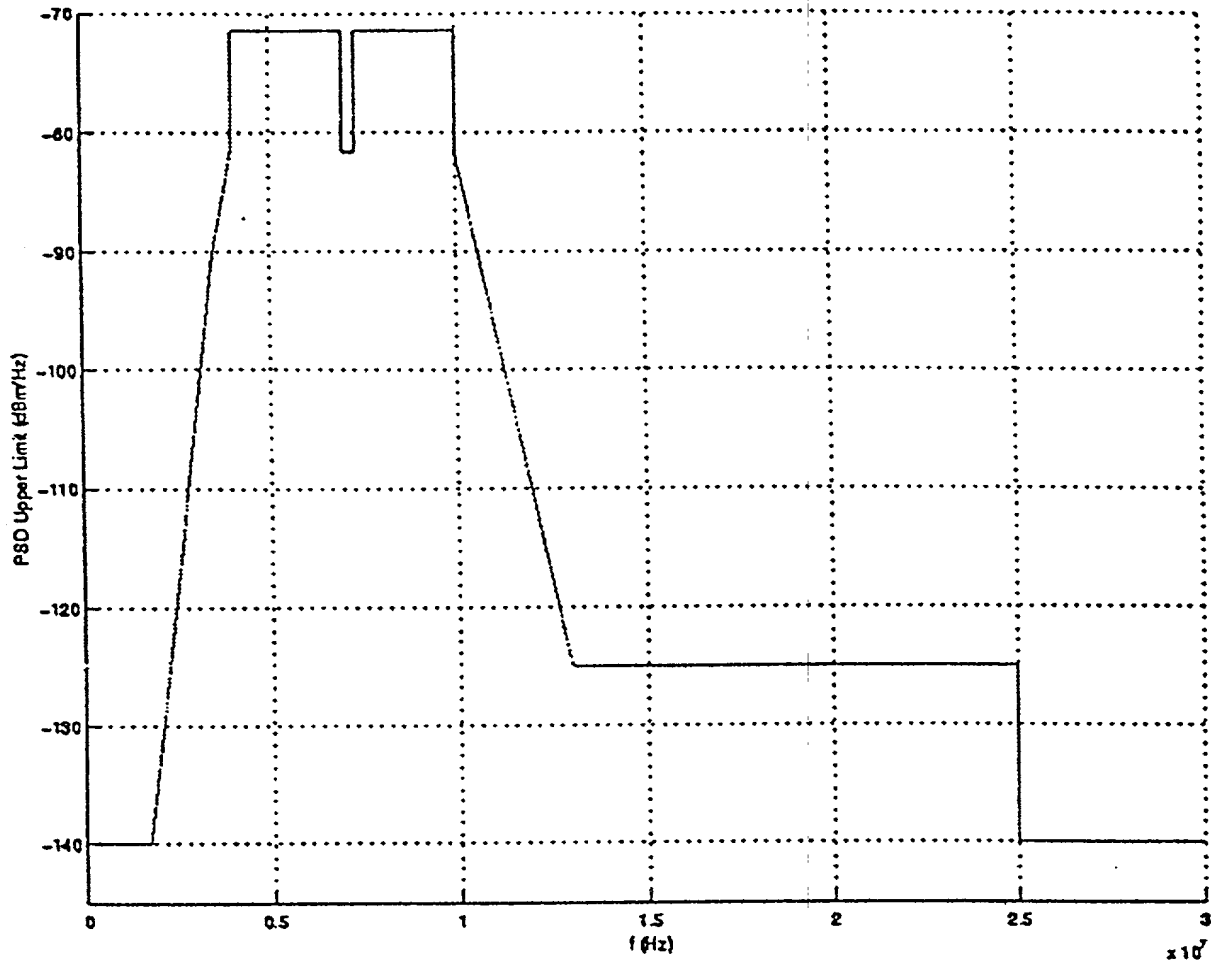


FIG. 23a

Frequency (MHz)	PSD Limit (dBm/Hz)
$0.015 < f \leq 1.7$	-140
$1.7 < f \leq 3.5$	$-140 + (f - 1.7) \cdot 50.0 / 1.8$
$3.5 < f \leq 4.0$	$-90 + (f - 3.5) \cdot 17.0$
$4.0 < f < 7.0$	-71.5
$7.0 \leq f \leq 7.3$	-81.5
$7.3 < f < 10.0$	-71.5
$10.0 \leq f < 13.0$	$-81.5 - (f - 10.0) \cdot 43.5 / 3.0$
$13.0 \leq f < 25.0$	-125
$25.0 \leq f < 30.0$	-140

FIG. 23b



Frequency Range (MHz)	Maximum Peak- to-Peak Interferer Level (Volts)
0.01 – 0.1	6.0
0.1 – 0.6	3.3
0.6 – 1.7	1.0
1.7 – 4.0	0.1
7.0 – 7.3	0.1
10.0 – 10.15	0.1
14.0 – 14.35	0.28
18.068 – 18.168	0.5
21.0 – 21.45	0.5
24.89 – 24.99	0.5
28.0 – 29.7	0.5

FIG. 25

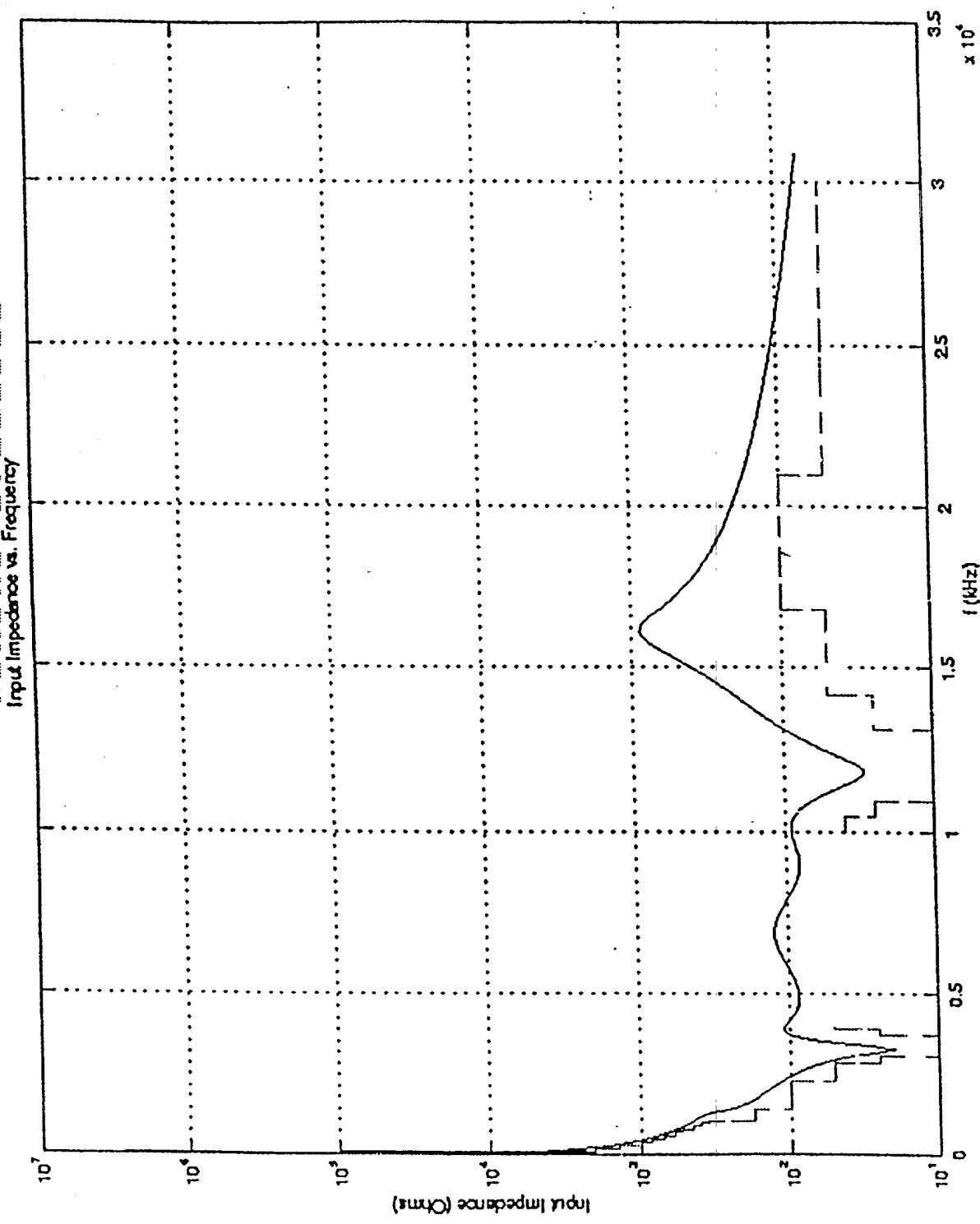
Frequency Range (MHz)	Maximum Peak- to-Peak Interferer Level (Volts)
0.01 – 0.1	20.0
0.1 – 0.6	20.0
0.6 – 1.7	10.0
1.7 – 4.0	2.5
7.0 – 7.3	2.5
10.0 – 10.15	2.5
14.0 – 14.35	5.0
18.068 – 18.168	5.0
21.0 – 21.45	5.0
24.89 – 24.99	5.0
28.0 – 29.7	5.0

FIG. 26

Frequency Range (kHz)	Min. Impedance (Ohms)
$0 < f \leq 0.285$	1 M
$0.285 < f \leq 2.85$	100 k
$2.85 < f \leq 28.5$	10 k
$28.5 < f \leq 95$	4.0 k
$95 < f \leq 190$	2.0 k
$190 < f \leq 285$	1.4 k
$285 < f \leq 380$	1.0 k
$380 < f \leq 475$	850
$475 < f \leq 570$	700
$570 < f \leq 665$	600
$665 < f \leq 760$	525
$760 < f \leq 855$	450
$855 < f \leq 950$	400
$950 < f \leq 1000$	350
$1000 < f \leq 1400$	175
$1400 < f \leq 2300$	100
$2300 < f \leq 2850$	50
$2850 < f \leq 3085$	25
$3085 < f \leq 3725$	10
$3725 < f \leq 3935$	25
$3935 < f \leq 4000$	50
$10000 < f \leq 10450$	40
$10450 < f \leq 10925$	25
$10925 < f \leq 13125$	10
$13125 < f \leq 14175$	25
$14175 < f \leq 16800$	50
$16800 < f \leq 21000$	100
$21000 < f \leq 30000$	50

FIG. 27

Input Impedance vs. Frequency  
 Frequency (kHz) x 10<sup>4</sup>  
 Input Impedance (Ohms)

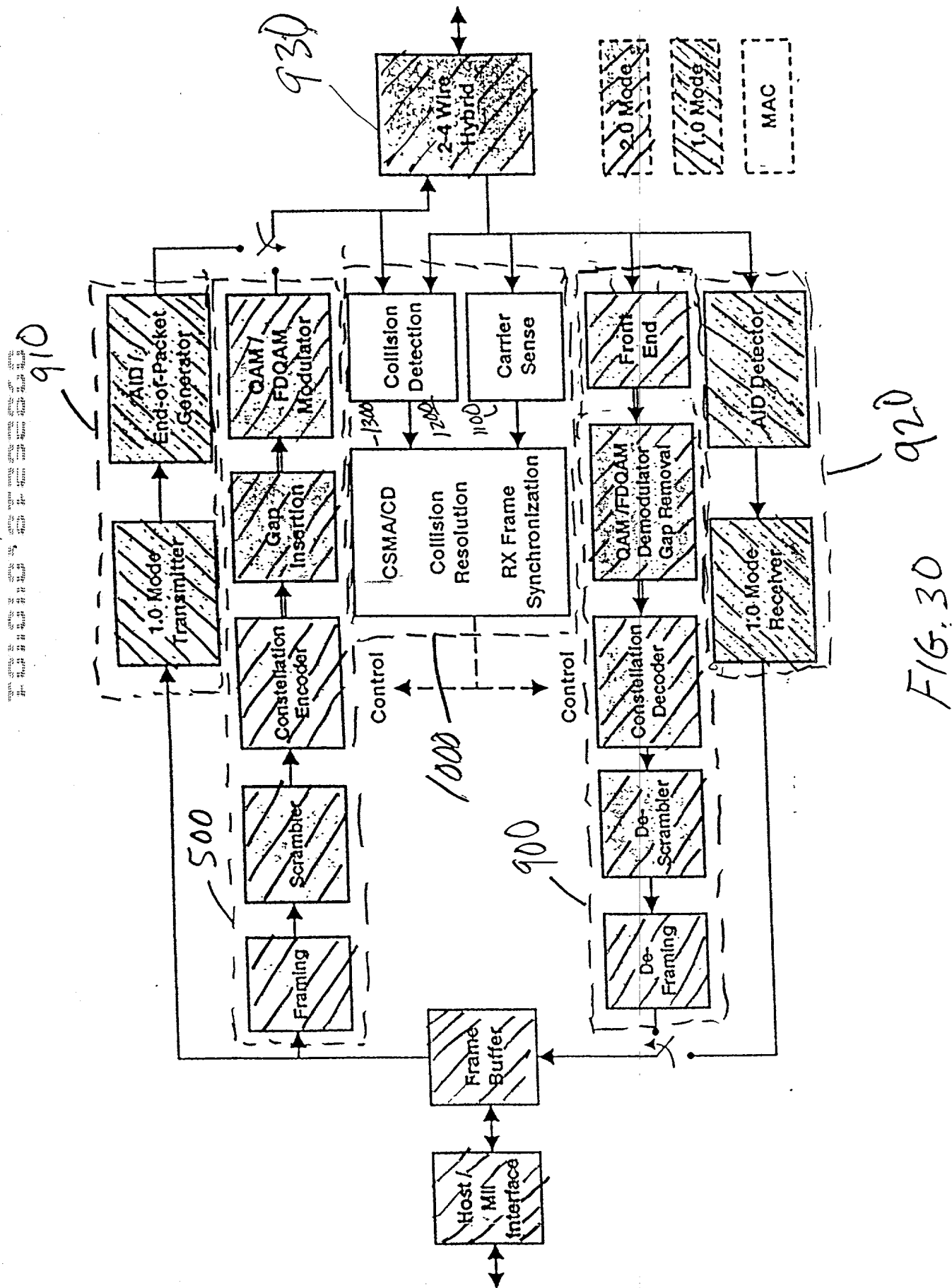


— INPUT IMPEDANCE  
 --- LOWER BOUND MASK

FIG. 28

OSI	IEEE	Function
DATA LINK	-	<b>Link Layer Signaling (driver)</b> a) Rate Adaptation, QoS and 1M8 Compatibility b) LARQ Error Recovery c) Link Integrity and Capability Discovery
	MAC Controller Layer	<b>MAC Controller Layer Functions</b> a) Host Interface b) Control and Status Registers, Interrupts c) DMA transfers, data buffering and command list interpretation d) Performance counters e) MAC address filtering, Wake-On-LAN processing
	MII	<b>Optional MII Interface (in PHY-only)</b>
	LLC - Logical Link Control	<b>Optional Link Layer Signaling (in PHY-only)</b> a) Rate Adaptation, QoS and 1M8 Compatibility b) Link Integrity and Capability Discovery
	MAC	<b>Frame Processing (transmit and receive)</b> a) Framing (frame boundary delineation and synchronization) b) Error detection (FCS generation and check, fragment detection)
	MAC	<b>Media Access Control (MAC)</b> a) CSMA/CD b) Collision Resolution (backoff algorithm)
PHY	PHY	<b>Physical Coding Sublayer</b> a) Coding and Modulation, Carrier Sense, Collision Detection

FIG. 29



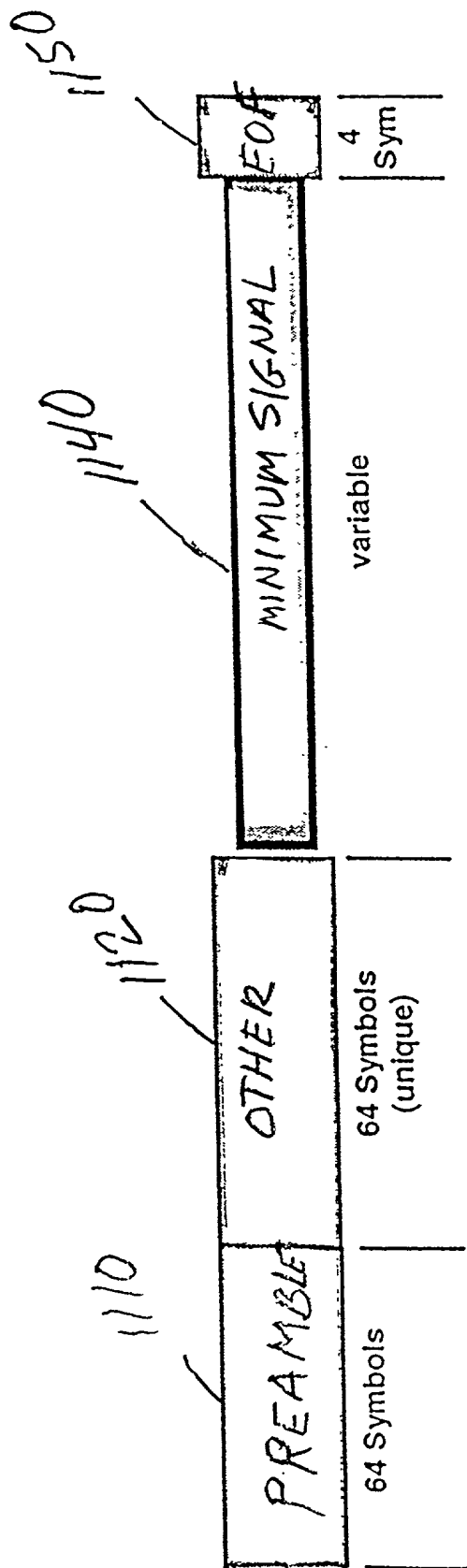


FIG. 31

FIG. 32 is a diagram illustrating a time slot structure for a transmission system. The diagram shows a sequence of time slots, each labeled with a priority (PRI) value. The slots are arranged in a row, with the first slot labeled PRI 7, followed by PRI 6, PRI 5, PRI 4, PRI 3, PRI 2, PRI 1, and PRI 0. A shaded rectangular area labeled TX is positioned at the beginning of the sequence, indicating the start of the transmission. A horizontal line with arrows at both ends represents the timeline. A vertical dashed line marks the start of the PRI 7 slot. A horizontal double-headed arrow labeled IFG (Inter-Fragment Gap) spans the duration of the PRI 7 slot. A vertical dashed line marks the end of the PRI 7 slot. A horizontal double-headed arrow labeled PRI\_SLOT MICROSECONDS spans the duration of the PRI 7 slot. A vertical dashed line marks the end of the PRI 7 slot. A horizontal double-headed arrow labeled 1400 spans the duration of the PRI 7 slot. A vertical dashed line marks the end of the PRI 7 slot. A horizontal double-headed arrow labeled 1700 spans the duration of the PRI 7 slot. A vertical dashed line marks the end of the PRI 7 slot.

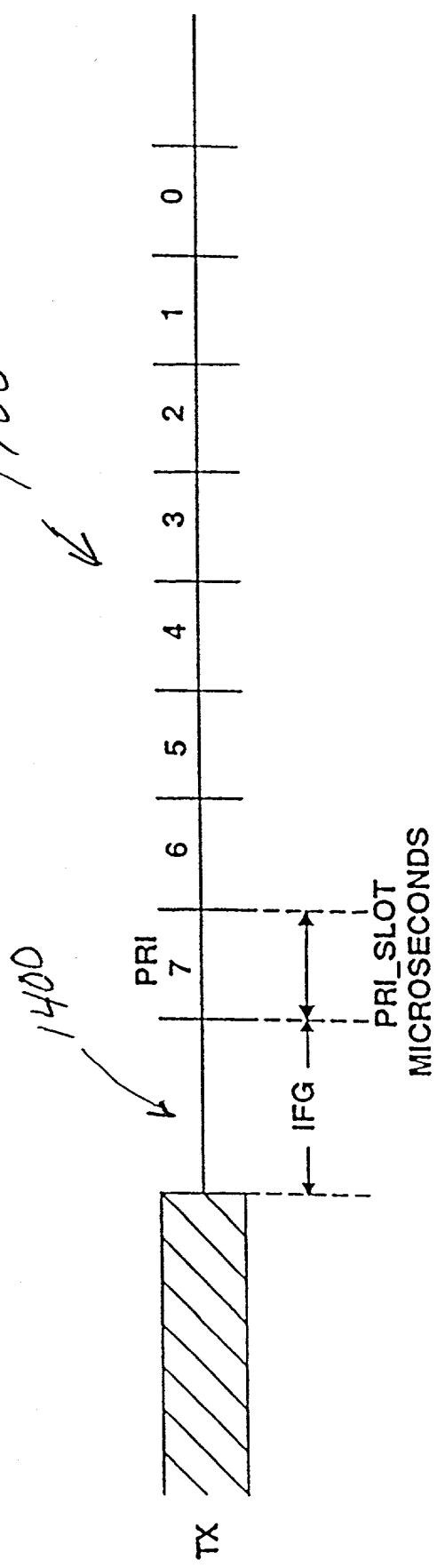


FIG. 32

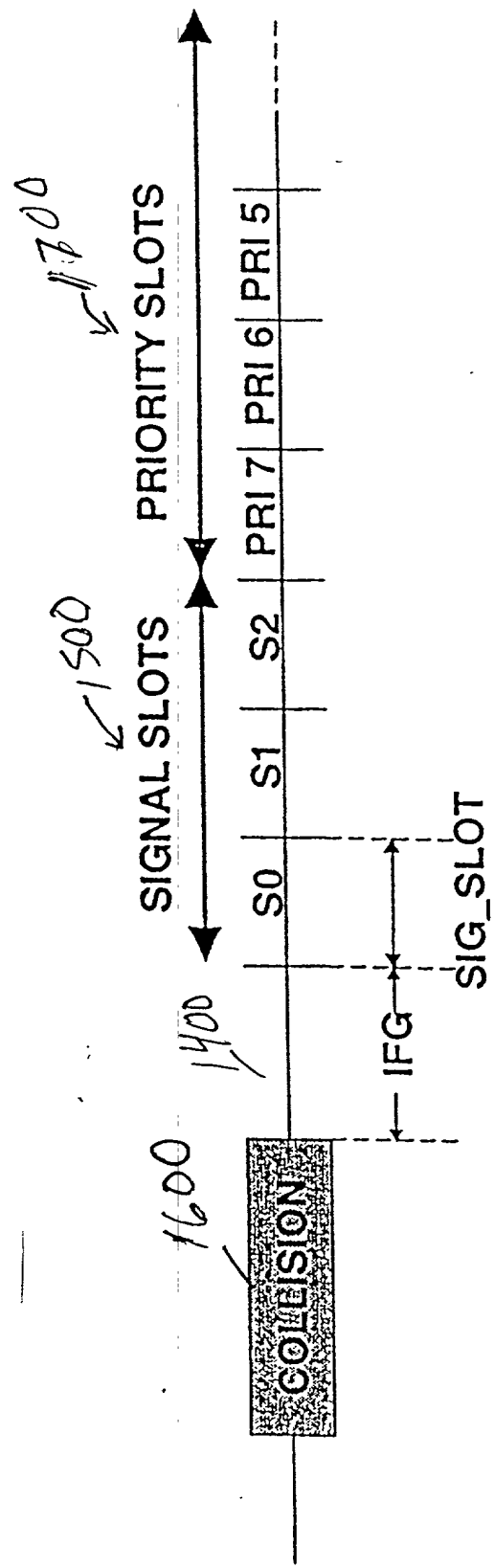


FIG. 33

FIG. 34a

Without Priority Access:

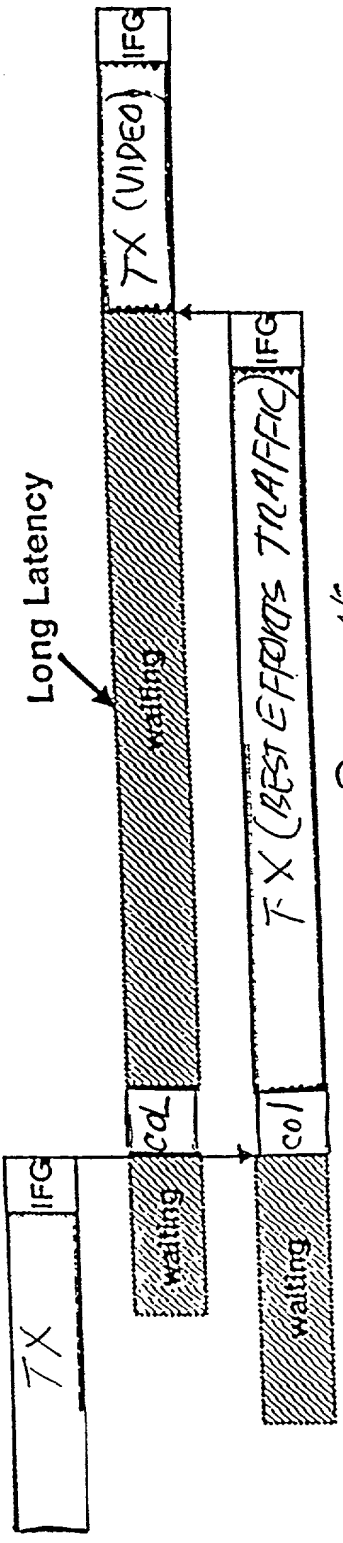


FIG. 34a

With Priority Access:

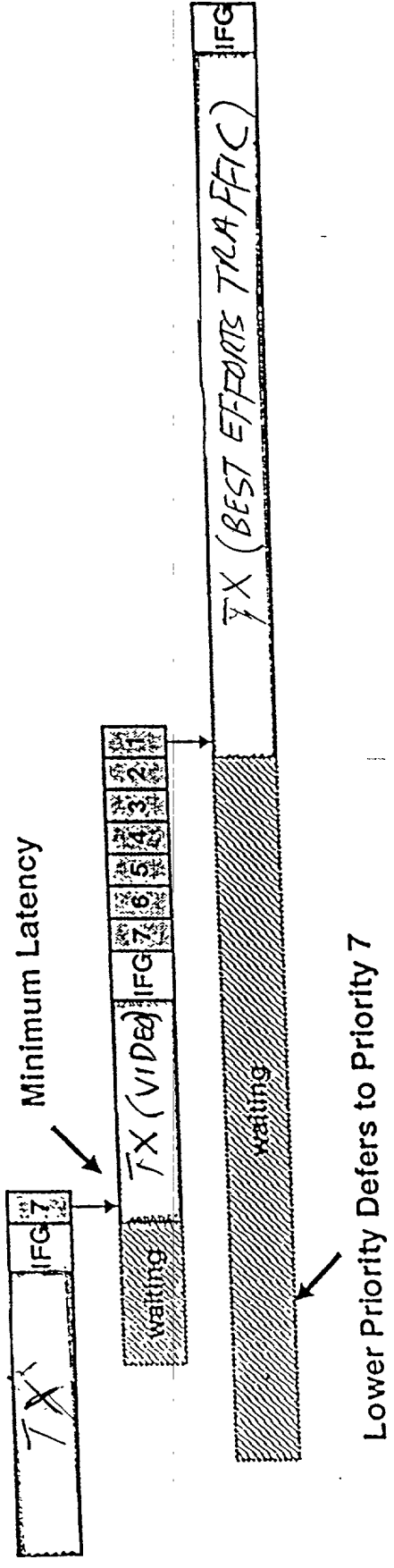


FIG. 34b

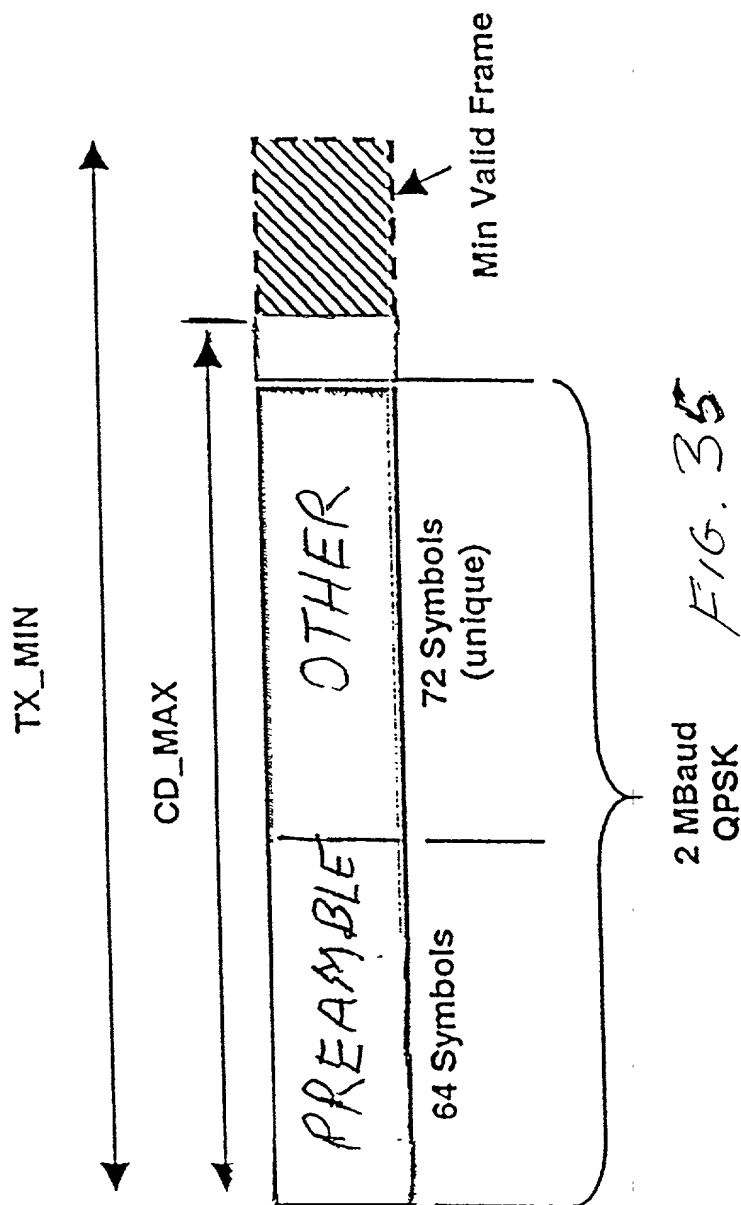


FIG. 35



Field	Length	Explanation
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Protocol Frame. Assigned to 8510 by IEEE)
SSType	1 octet	0 - Reserved 1 - Rate Request Control Frame 2 - Link Integrity Short Frame 3 - Capabilities Announcement 4 - LARQ 5 - Vendor-specific short format type 6 - 126 Reserved 127 Reserved Values 128-255 correspond to the Long Subtype
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field (or the first octet following SSLength if it is not defined as SSVersion) and ending with the second(last) octet of the Next EtherType field. Min is 2 and max is 255.
SSVersion	1 octet	Version number of the control information
Data	0-252 octets	Control information
Next EtherType	2 octets	EtherType/length of next layer protocol, 0 if none.
Pad	41-0 octets	Padding required to meet minimum if data < 41 octets
FCS	4 octets	Frame Check Sequence

Fig. 37

Field	Length	Explanation
DA	6 octets	Destination Address
SA	6 octets	Source Address
EtherType	2 octets	0x886c (Link Protocol Frame. Assigned to Epigram by IEEE)
LSType	2 octets	32768 Reserved 32769 Vendor-specific long-format 32770 - 65534 reserved 65535 Reserved
LSLength	2 octets	Number of additional octets in the control header, starting with the SSVersion field (or the first octet following SSLength if it is not defined as SSVersion) and ending with the second(last) octet of the Next Ethertype field. Min is 2 and max is 65535.
LSVersion	1 octet	Version number of the following protocol information.
Data	LSLength - 3 octets	LSType protocol dependent data
Next Ethertype	2 octets	Ethertype/length of next layer protocol, 0 if none.
Pad	42-0 octets	pad to minimum size if needed
FCS	4 octets	Frame Check Sequence

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Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Control Frame)
SSType	1 octet	=1
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next EtherType field. The minimum value of SSLength is 8 for SSVersion 0.
SSVersion	1 octet	=0
OpCode	1 octet	Operation code for this control message.
NumBands	1 octet	Number of bands specified in this control. Each band has a two octet descriptor. The first band refers to 2 MBaud modulation rate, the next to 4 MBaud. NumBands shall be 1 or 2 on transmission for 10M8 stations, and stations shall ignore band entries beyond Band2 on receive if NumBands is larger than 2. The value 0 is not allowed.
NumAddr	1 octet	Number of addresses specified in the payload of this control message. NumAddr may be zero. The SA in the Ethernet header is always used, and is referred to in the following sections as RefAddr0.
Band1_PE	1 octet	2MBaud, 7 MHz carrier : The PE value that should be used to send data when the 2MBaud band is selected. (1..8) are the only valid values. The value 8 is used to request HPNA 1.0 type frames, and is valid only when the network is operating in VIM2mode, and only in Band1.
Band1_rank	1 octet	The rank order of the ReqDAs' preference for this band, 1 is highest preference, and the other bands are assigned successively larger rank values, no two bands shall have the same rank
<del>Band2_PE</del>	<del>1 octet</del>	<del>Optional, only present if NumBands &gt;= 2. 4MBaud, 7 MHz carrier: If included, this field is the PE value that should be used to send data when the 4MBaud band is selected. (0, 9..15) are the only valid values.</del>
<del>Band2_rank</del>	<del>1 octet</del>	<del>Optional, only present if NumBands &gt;= 2. Rank order of ReqDAs' preference for this band</del>
<del>RefAddr1</del>	<del>6 octets</del>	<del>Optional. Present if NumAddr &gt;= 1. The second MAC Address for which the rates are being specified, typically Broadcast or a multicast address.</del>
<del>RefAddr2</del>	<del>6 octets</del>	<del>Optional. Present if NumAddr &gt;= 2. The third MAC Address for which the rates are being specified.</del>
<del></del>		<del>[additional instances of RefAddr, until the number of RefAddr fields equals NumAddr]</del>
Next EtherType	2 octets	=0.
Pad		To reach minFrameSize if required
FCS	4 octets	Frame Check Sequence

FIG. 39

PE	Data Rate	Meaning
0	N/A	Means this band is Not Supported
1	4 Mbit/s	2 Mbaud FDQAM, 2 bits per Baud
2	6 Mbit/s	2 Mbaud FDQAM, 3 bits per Baud
3	8 Mbit/s	2 Mbaud FDQAM, 4 bits per Baud
4	10 Mbit/s	2 Mbaud FDQAM, 5 bits per Baud
5	12 Mbit/s	2 Mbaud FDQAM, 6 bits per Baud
6	14 Mbit/s	2 Mbaud FDQAM, 7 bits per Baud
7	16 Mbit/s	2 Mbaud FDQAM, 8 bits per Baud
8	1 Mbit/s	HPNA 1.0
9	8 Mbit/s	4 Mbaud QAM, 2 bits per Baud
10	12 Mbit/s	4 Mbaud QAM, 3 bits per Baud
11	16 Mbit/s	4 Mbaud QAM, 4 bits per Baud
12	20 Mbit/s	4 Mbaud QAM, 5 bits per Baud
13	24 Mbit/s	4 Mbaud QAM, 6 bits per Baud
14	28 Mbit/s	4 Mbaud QAM, 7 bits per Baud
15	32 Mbit/s	4 Mbaud QAM, 8 bits per Baud

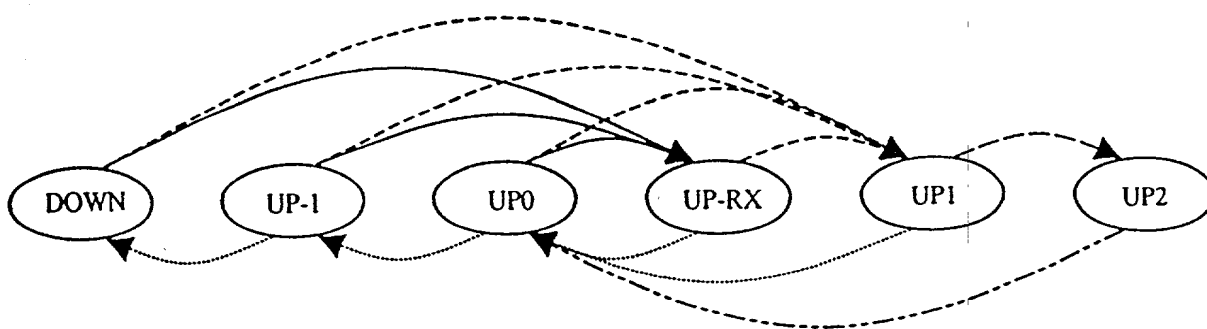
FIG. 40

OpCode	Meaning
0	Rate Change Request
1	Rate Test Request
2	Rate Test Reply
3-255	Reserved

FIG. 41

<b>band specification</b>	A Payload Encoding (PE) and Rank associated with a given band. A band is a single combination of baud rate, modulation type (e.g. QAM or FDQAM) and carrier frequency. Two bands are defined in <i>HPNA V2</i>
<b>Logical channel, channel</b>	A flow of frames from a sender to one or more receivers on a single network segment, consisting of all the frames with a single combination of DA and SA.
<b>Receiver</b>	A station that receives frames sent on a particular channel. If the destination is a unicast address there is at most one receiver. If the destination is a group address (including broadcast), there may be many receivers.
<b>Receiver PE</b>	The preferred PE to be used on this channel, as determined by the receiver.
<b>RRCF</b>	Rate Request Control Frame. Sent from the receiver to the sender to effect a change in PE.
<b>RefAddr0</b>	The SA in the Ethernet header of the RRCF frame. This is the DA of the receiver (for the channel), and is always used by the channel sender as the first RefAddr processed.
<b>RefAddr1..RefAddr&lt;n&gt;</b>	Other addresses including Broadcast and Multicast addresses for which the receiver is indicating rate information to the sender. The channel receiver's station address (RefAddr0) should not be put in the list of additional RefAddr's.  Note1: At least one RefAddr field is necessary to support rate negotiation for Broadcast and Multicast addresses since these cannot be used as the source address in the Ethernet header.
<b>Sender</b>	The sending station for a channel, usually the station owning the source MAC address.
<b>Sender PE</b>	The preferred PE associated with a channel, as noted by the sender.

*FIG. 42*



- > Receive any non-broadcast frame or link indication
- - - -> Receive a frame with DA == Broadcast (0xFFFFFFFF) – Set SA1 = SA
- .....> Receive a frame with DA == Broadcast (0xFFFFFFFF) and SA != SA1
- > Timeout of 1 second free-running timer – Send LICF, reinitialize Force\_Send
- - - -> Timeout - If Force\_Send == 0 then Send LICF, reinit Force\_Send else decrement Force\_Send

FIG. 43a

	DOWN	UP-1	UP0	UP-RX	UP1	UP2
Receive 1.0 link indication or any non-broadcast frame	UP-RX (none)	UP-RX (none)	UP-RX (none)	UP-RX (none)	UP1 (none)	UP2 (none)
Receive broadcast frame with SA == SA1	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 (none)	UP2 (none)
Receive broadcast frame with SA != SA1	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	UP1 Set SA1<-SA	Native:UP2 Compat: UP1 (none)	UP2 (none)
Timeout and Force_Send == 0	DOWN Send LICF, reinit Force_Send	DOWN Send LICF, reinit Force_Send	UP-1 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send
Timeout and Force_Send > 0	DOWN Send LICF, reinit Force_Send	DOWN Send LICF, reinit Force_Send	UP-1 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 Send LICF, reinit Force_Send	UP0 decrement Force_Send

FIG. 43b

Field	Length	Meaning
DA	6 octets	Destination Address (FF:FF:FF:FF:FF:FF)
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
SSType	1 octet	=2
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Etherthertype field. Minimum is 4 for SSVersion 0.
SSVersion	1 octet	=0
LI_pad	1 octet	Ignored on reception.
Next Etherthertype	2 octets	=0
Pad	41 octets	Any value octet
FCS	4 octets	

FIG. 44

Field	Length	Meaning
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address of the station that transmitted this frame
Ethertype	2 octet	0x886c (Link Control Frame)
SSType	1 octet	=3
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next EtherType field. Minimum is 32 for SSVersion 0
SSVersion	1 octet	=0
CSA_ID_Space	1 octet	Identifies the registration space of CSA_MFR_ID 0 – Unspecified 1 – JEDEC 2 – PCI
CSA_MFR_ID	2 octets	HW manufacturer ID - Identifies the manufacturer of the PHY controller chip. The purpose of this field plus the part number and revision is to identify specific implementations of the PHY specification. This is not a board or assembly-level identifier.
CSA_Part_No	2 octets	HW Manufacturer Part Number - The part number of the PHY controller chip.
CSA_Rev	1 octet	HW Revision
CSA_Opcode	1 octet	0 – Announce 1 – Request
CSA_MTU	2 octets	Maximum size link-level PDU this receiver accepts in octets, the default value is 1526 octets. This is also the minimum value that shall be accepted by all ILINE10 stations
CSA_SA	6 octets	Source address of the station that generated this CSA frame
CSA_pad	2 octets	Reserved for version 0. Shall be sent as 0, ignored on reception.
CSA_CurrentTxSet	4 octets	Configuration flags, plus all current in-use status for this station.
CSA_OldestTxSet	4 octets	A copy of the "oldest" TX flags for this stations, from the period ending at least one period(minute) earlier.
CSA_CurrentRxSet	4 octets	The union of recent flags received from other stations.
Next EtherType	2 octets	=0
Pad		Pad to reach minFrameSize if necessary
FCS	4 octets	

FIG. 45

Octet	Field	Length	Description
Flags0	TxPriority7	1	Station is(was) transmitting frames with LL priority 7. (always set)
	TxPriority6	1	Station is(was) transmitting frames with LL priority 6.
	TxPriority5	1	Station is(was) transmitting frames with LL priority 5.
	TxPriority4	1	Station is(was) transmitting frames with LL priority 4.
	TxPriority3	1	Station is(was) transmitting frames with LL priority 3.
	TxPriority2	1	Station is(was) transmitting frames with LL priority 2.
	TxPriority1	1	Station is(was) transmitting frames with LL priority 1.
	TxPriority0	1	Station is(was) transmitting frames with LL priority 0. (always set)
Flags1	Reserved	6	Shall be sent as 0 and ignored by 2.0 stations when received.
	No_V1M2_Frames	1	This station does not support the reception or transmission of compatibility frames (V1M2 frames).
	Supports 4Mbaud	1	This station supports 4 megabaud payload encodings.
	Reserved	8	Shall be sent as 0 and ignored by 2.0 stations when received.
Flags2	ConfigV2	1	Force use of 10M8 mode, defers to Config1 and ConfigV1M2.
	ConfigV1M2	1	Force use of V1M2 mixed mode, defers to ConfigV1.
	ConfigV1	1	Force use of HPNA 1.x mode, highest precedence of config flags.
	Reserved	2	Shall be sent as 0 and ignored by 2.0 stations when received.
	Highest Version	3	This station's highest supported HPNA version:
			0x000 – Reserved
Flags3			0x001 – HPNA1.0
			0x010 – iLine10
			0x011-0x111 Reserved

FIG. 46

DeleteSet	A computed value used to detect newly removed status information.
NewRxFlags, ReallyNewRxFlags	Computed values used to detect new status flags.

FIG. 47

CSP_Timer	A free-running timer with a period of 60 seconds.
RetransmitTimer	A one-shot timer, set to a random interval in the range 1 ms to 1000 ms, inclusive, after sending a CSA in which CSA_CurrentTxSet and CSA_OldestTxSet are different, or when a CSA is received with the CSA_Opcode set to 1 (Request). This timer is cancelled if a second CSA is sent as a result of the CSP_Timer expiring.

FIG. 48

NewTxSet	The set of flags announced during the current CS period, updated immediately when a new link layer priority is used or new volatile status is set. When the CSP_Timer expires, CurrentTxSet is given the value of NewTxSet, and NewTxSet is reset to the default set.
PreviousTxSet	The set of flags that were announced during the previous CS period (the ending value of NewTxSet from the previous CS period).
OldestTxSet	The set of flags rolled over from PreviousTxSet at the end of the previous CS period (the value of PreviousTxSet from the previous CS period). Flags that are present in OldestTxSet and missing from PreviousTxSet were not actively used or detected (by the sender) for an entire CS period, and will be deleted. This set is sent in CSA frames as CSA_OldestTxSet.
NewRxSet	<p>The union of all CSA_CurrentTxSet flags received in CSAs from other stations during the current CS period. This is rolled over into PreviousRxSet at the expiration of the CSP_Timer, then reset to the empty set (0).</p> <p>A volatile status flag (one of the priority flags) in this set may subsequently be deleted if the only station previously announcing that flag stops using it. The deletion from that station's CurrentTxSet is noted by the difference from its OldestTxSet. The fact that it was the only sender is noted by the absence of the flag in that station's CurrentRxSet, indicating that it has received the flag from no other stations.</p> <p>If deleted from NewRxSet, a flag shall also be deleted from PreviousRxSet.</p>
PreviousRxSet	The set of announced flags received during the previous CS period (the ending value of NewRxSet from the previous CS period). A flag may be deleted from this set, as described under NewRxSet above.

FIG. 49

CurrentTxSet	The set of flags that were announced during the previous CS period plus any new status and priority flags (or changed configuration/options flags) used during the current CS period, i.e. the union of PreviousTxSet and NewTxSet. This set is sent in CSA frames as CSA_CurrentTxSet.
CurrentRxSet	The union of NewRxSet, PreviousRxSet. This set is sent in CSA frames as CSA_CurrentRxSet.
CurrentInUseSet	The union of CurrentTxSet and CurrentRxSet. This set is used to determine the operational mode of the station and to modify the mapping between the LL priority of the frame and the actual PHY priority usage.

Fig. 50

TX LL priority							
0	1	2	3	4	5	6	7
Default TX Phy Priorities							
2	0	1	3	4	5	7	6

FIG. 51a

TX LL priority							
0	1	2	3	4	5	6	7
Remapped TX Phy Priorities							
CurrentInuse Priorities (LL)							
0							7
0						6	7
0	1			4			7
0			3		5	6	7

FIG. 51b

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Control Frame)
SSType	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 6 for SSVersion 0.
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Control Header data with LARQ_ctl bit = 1, LARQ_NACK = 0.
Next Ethertype	2 octets	=0
Pad	38 octets	
FCS	4 octets	Frame Check Sequence

FIG. 52a

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (Link Control Frame)
SSType	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 12 for Nack frames with SSVersion 0.
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Control Header data with LARQ_ctl bit = 1, LARQ_NACK = 1..7.
NACK_DA	6 octets	Original Destination Address
Next Ethertype	2 octets	=0
Pad	32 octets	
FCS	4 octets	Frame Check Sequence

FIG. 52b

Field	Length	Meaning
DA	6 octets	Destination Address (from original Ethernet PDU)
SA	6 octets	Source Address (from original Ethernet PDU)
Ethertype	2 octets	0x886c (Link Control Frame)
SStype	1 octet	=4
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next Ethertype field. SSLength is 6 for SSVersion 0.=6
SSVersion	1 octet	=0
LARQ_hdr data	3 octets	LARQ Encapsulation header data (with LARQ_CTL bit = 0)
Next Ethertype	2 octets	From original Ethernet PDU
Payload	Min 46 octets	From original Ethernet PDU payload
FCS	4 octets	Frame Check Sequence

FIG. 52c

Octet	Field	Length	Meaning
Flags0	LARQ_Mult	1 bit	Multiple Retransmission Flag. 0 in the original transmission of a data frame. For retransmitted frames (LARQ_Rtx = 1), set to the value of LARQ_Mult in the NACK-frame that caused the retransmission. This flag can be used by receivers to measure the round-trip times associated with the miss/nack/receive-rtx process.
	LARQ_Rtx	1 bit	0 for first transmission of a frame, 1 if frame is retransmitted. Stations not implementing LARQ shall drop any data frame if this bit is 1.
	LARQ_NoRtx	1 bit	0 if implementation supports retransmission, 1 if only priority is meaningful. May be used on a per-channel basis.
	LARQ_NewSeq	1 bit	1 if the sequence number space for the channel has been reset, and older sequence numbers should not be nacked, 0 otherwise
	LARQ_Ctl	1 bit	"0" when in Encapsulation Format
	Priority	3 bits	Link Layer Priority of this frame
Flags1_Seq0	Reserved	4 bits	Reserved, shall be 0
	LARQ_seq_high	4 bits	High 4 bits of Sequence number
Seq1	LARQ_seq_low	8 bits	Low 8 bits of Sequence number

FIG. 52d

Octet	Field	Length	Meaning
Flags0	LARQ_Mult	1 bit	Multiple Retransmission Flag. 0 in the first Nack sent for a given sequence number, 1 in all retransmitted Nacks.
	LARQ_NACK	3 bits	NACK Count If 0 in a LARQ Control Frame, then this is a Reminder.
	LARQ_Ctl	1 bit	Set to 1 for LARQ Control Header data format
	Priority	3 bits	Link Layer Priority of this frame
Flags1_Seq0	Reserved	4 bits	Reserved, shall be 0
	LARQ_seq_high	4 bits	High 4 bits of Sequence number
Seq1	LARQ_seq_low	8 bits	Low 8 bits of Sequence number

FIG. 52c

<b>Control frame</b>	A frame generated by a LARQ protocol module that contains only a LARQ protocol header as its payload.
<b>Current sequence number</b>	The most recently received new sequence number for a channel.
<b>Data frame</b>	Any standard Ethernet frame from higher (than LARQ) protocol layers. A LARQ-enabled station encapsulates the original payload of an Ethernet frame by inserting a LARQ header (short form control header with LARQ_hdr data) between the source address and the remainder of the frame before the frame is passed down to the driver for transmission on the network.
<b>Forget timer</b>	An implementation dependent mechanism to allow a receiver to reset the sequence number space of a channel when a received sequence number is not the next expected ( <b>Current Sequence Number + 1</b> ). One second is a suggested default value.
<b>Hold timer, lost timer</b>	An implementation dependent timing mechanism that limits the time a receiver will hold onto a received frame while waiting for a missing frame to be retransmitted. Conceptually, there is one such timer per missing sequence number. The timer interval is <b>Maximum Hold Interval</b> .
<b>Logical channel, channel</b>	A flow of frames from a sender to one or more receivers on a single network segment consisting of all the frames with a single combination of destination address, source address, and link layer priority.
<b>NACK, Nack, nack</b>	An indication from a receiver to a sender requesting retransmission of one or more frames. Also, the action of providing such an indication. E.g. "to nack a sequence number" meaning to send a NACK indication.
<b>NACK timer</b>	An implementation dependent timing mechanism used by a receiver to retransmit NACKs for missing sequence numbers. Conceptually, there is one such timer per missing sequence number per <b>logical channel</b> . The timer is reset each time a NACK is sent for a sequence number. The timer interval is <b>NACK Retransmission Interval</b> .
<b>new</b>	A new sequence number is one whose difference from the <b>current sequence number</b> for the channel, modulo the size of the sequence number space and considered as a signed integer, is greater than 0. In particular, the numbers (current + 1) through (current + 2047).
<b>old</b>	An old sequence number is one whose difference from the <b>current sequence number</b> for the channel, modulo the size of the sequence number space and considered as a signed integer, is less than or equal to 0. In particular, the numbers (current - 2048) through (current) are old. Note, however, that most of the old sequence numbers are also out-of-sequence.

Fig. 52f.1

<b>out of sequence</b>	Any sequence number that falls outside a reasonable range, old or new, of the current sequence number for a logical channel is considered out of sequence. It is recommended that plus or minus twice the value of MaximumSaveLimit (defined below) be used as the "reasonable range" when checking for out of sequence.
<b>receiver</b>	A station that receives frames sent on a particular channel. If the destination address is a unicast address there is at most one receiver. If the destination address is a group address (including broadcast), then there may be many receivers.
<b>reminder</b>	A control frame sent by the channel <b>sender</b> with the most recently used sequence number for a channel which has been inactive for <b>Reminder Interval</b> after its most recent data frame.
<b>reminder timer</b>	An implementation dependent timing mechanism used by a sender to generate a reminder frame after a period of inactivity for a channel. The timer is reset each time a new data frame is transmitted. Conceptually, there is one such timer per channel. The timer interval is <b>Reminder Interval</b> .
<b>save timer</b>	An implementation dependent timing mechanism that limits the time a sender will save a frame waiting for retransmission requests. The timer interval is <b>Maximum Save Interval</b> .
<b>sender</b>	The sending station for a channel, usually the station owning the source MAC address.
<b>sequence numbers</b>	Sequence numbers are maintained separately for each logical channel by the sender.

FIG. 52f.2

<b>Send Sequence Number</b>	The sequence number of the most recently transmitted data frame.
<b>Reminder Timer Interval</b>	A fixed interval. The default is 50 ms. Lower values will increase the overhead of reminders on network load, while higher values increase the latency for end-of-sequence frames requiring retransmission. Implementations should not use values outside of the range 25-75 ms, based on 150 ms maximum save and hold times.
<b>Minimum Retransmission Interval</b>	An interval used to prevent too-frequent retransmissions of a single frame. Most important for multicast channels. The default is 10 ms.
<b>Maximum Save Limit</b>	The maximum number of frames that will be saved for a single logical channel. This is implementation dependent, and varies with the maximum frame rate the sender is expected to support. Values of 100 or more can be useful for high-speed applications such as video.
<b>Maximum Save Interval</b>	The maximum time that the sender will normally save a frame for possible retransmission. The default is 150 ms.

FIG. 53

<b>Current Sequence Number</b>	The most recent sequence number received in a LARQ header for the channel, whether in a data frame or a reminder control frame.
<b>Oldest missing sequence number</b>	The oldest sequence number for a frame not yet received which has not been declared lost.
<b>Maximum Hold Interval</b>	The longest interval that a frame will be held awaiting an earlier missing frame. The default is to use the same value as <b>Maximum Save Interval</b> , which has a default of 150 ms
<b>Maximum Receive Limit</b>	The maximum number of frames that a receiver will buffer while awaiting an earlier missing frame. The default should normally be the same as the <b>Maximum Save Limit</b> .
<b>NACK Retransmission Interval</b>	The interval after which a receiver will retransmit a Nack control frame for a missing sequence number, with the expectation that earlier Nack control frames or data frame retransmissions were lost. The default for fixed implementations is 20 ms.

FIG. 54

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
SSType	1 octet	=5
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second(last) octet of the Next EtherType field. SSLength shall be >= 6 for SSVersion 0.
SSVersion	1 octet	=0
Vendor OUI	3 octets	An IEEE assigned Organizationally Unique Identifier
Control data	0-249 octets	Vendor specific control data
Next EtherType	2 octets	= next EtherType if an encapsulation format, or 0 if no encapsulated frame
Pad	0-38 octets	Any value octet
FCS	4 octets	

FIG. 55a

Field	Length	Meaning
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octet	0x886c (Link Control Frame)
LSType	2 octets	= 32769
LSLength	2 octets	Number of additional octets starting with the LSVersion field and ending with the second(last) octet of the Next EtherType field. LSLength shall be > 6 for LSVersion 0.
LSVersion	1 octet	=0
Vendor OUI	3 octets	An IEEE assigned Organizationally Unique Identifier
Control data	1-65531 octets	Vendor specific data
Next EtherType	2 octets	= next EtherType if an encapsulation format, or 0 if no encapsulated frame
Pad	40-0 octets	If needed to make minimum size frame. Should be zero
FCS	4 octets	

FIG. 55b

carrier sense state	Output events
init	energy $\leq 0$ . Only start-of-preamble events checked.
idle	Only start-of-preamble events checked.
busy	Only end-of-preamble events checked.
transmit	Only start-of-preamble events checked (collision detection).

FIG. 56

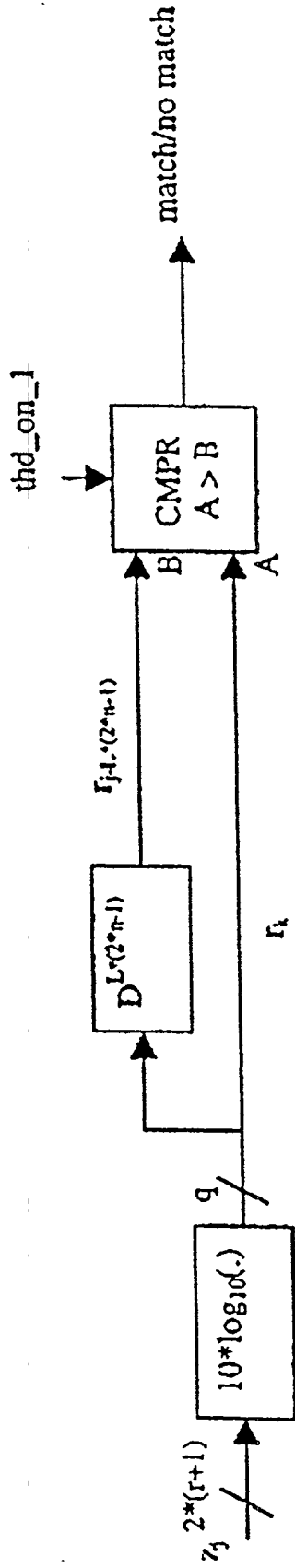


FIG. 57

2022

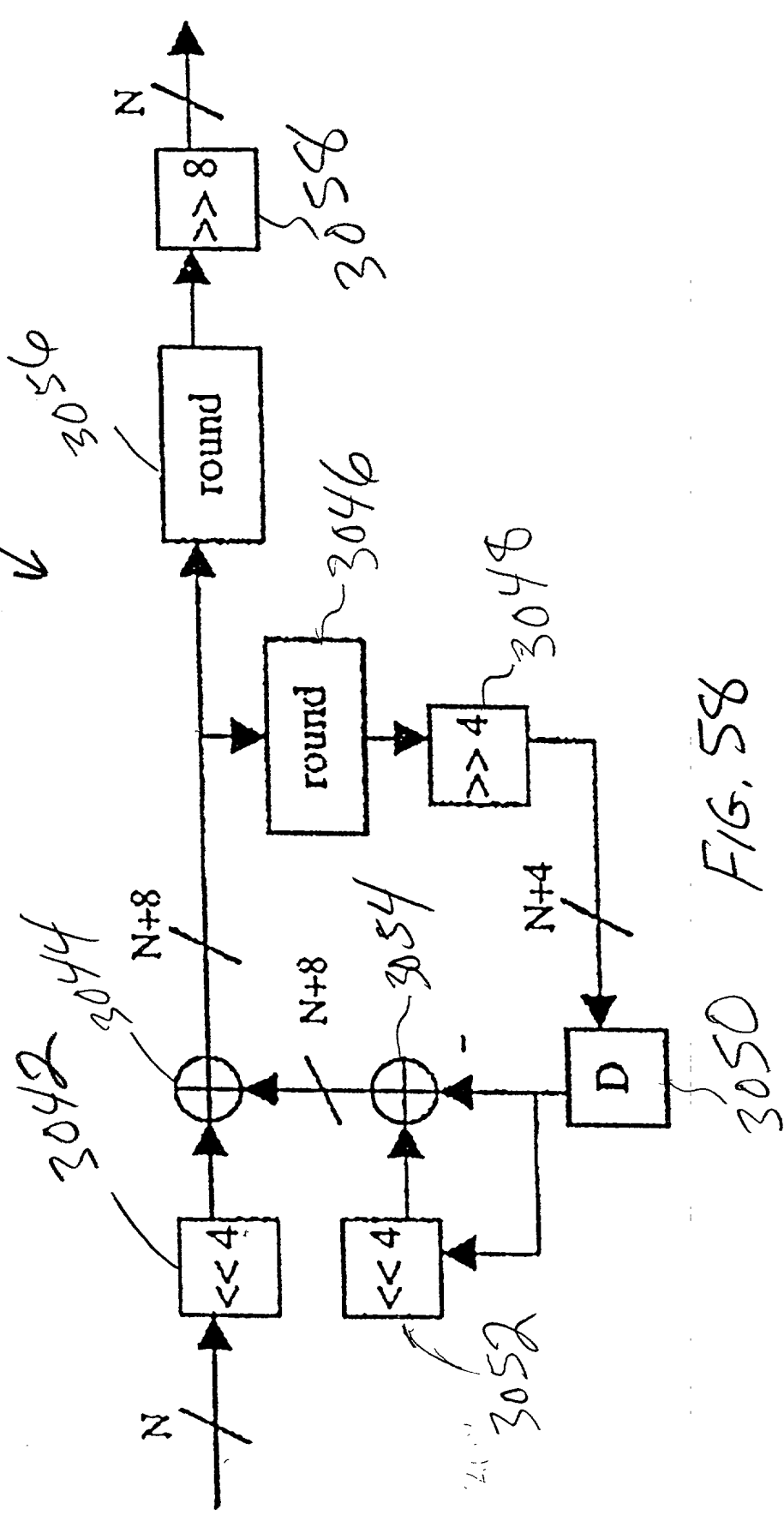


FIG. 58

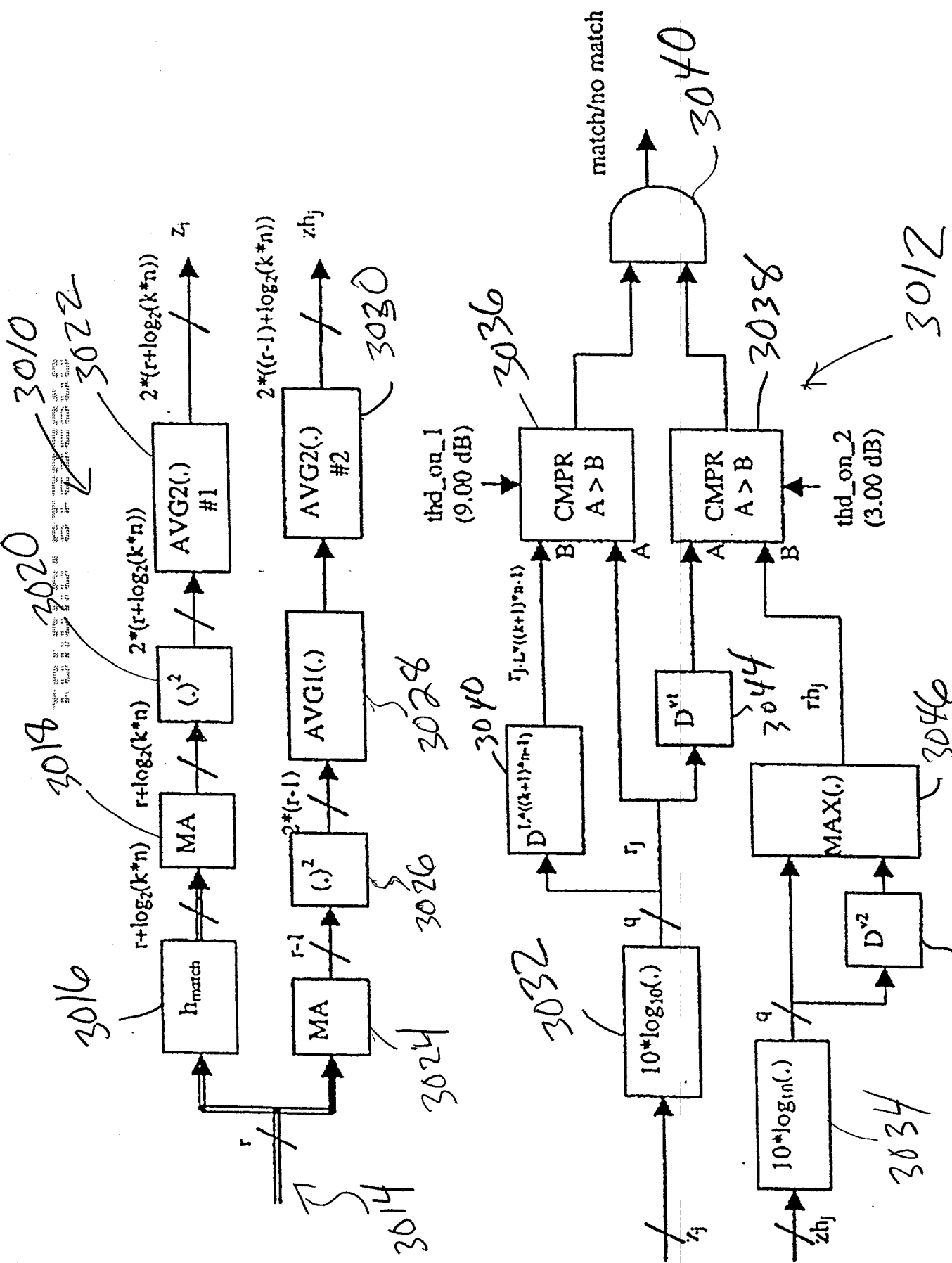


FIG. 59

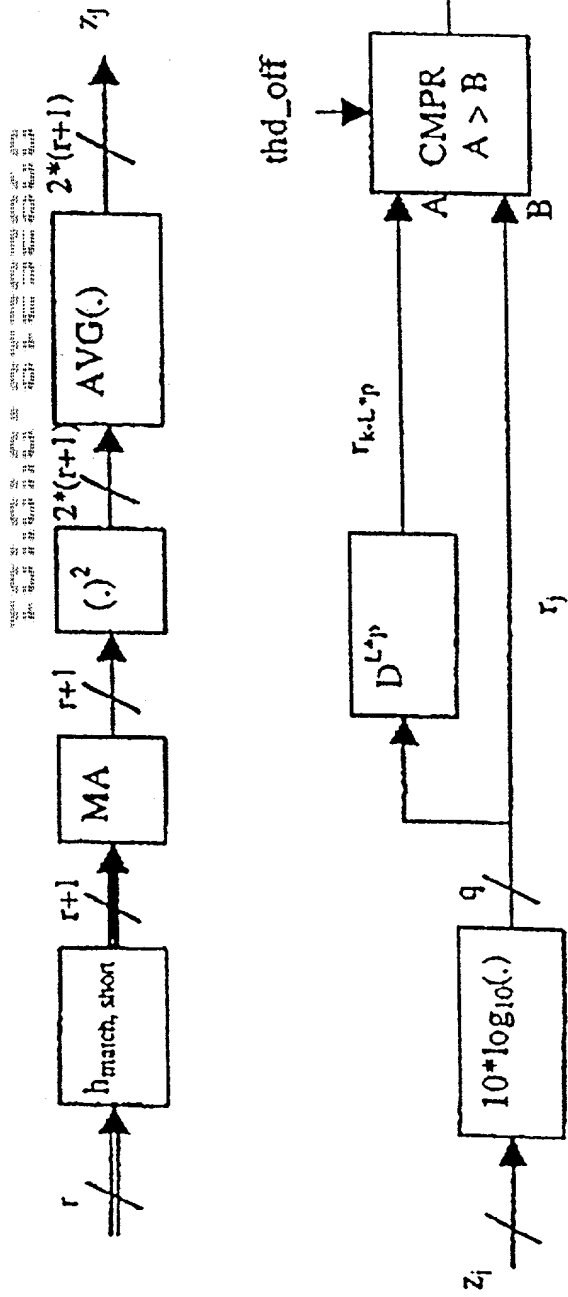


FIG. 60

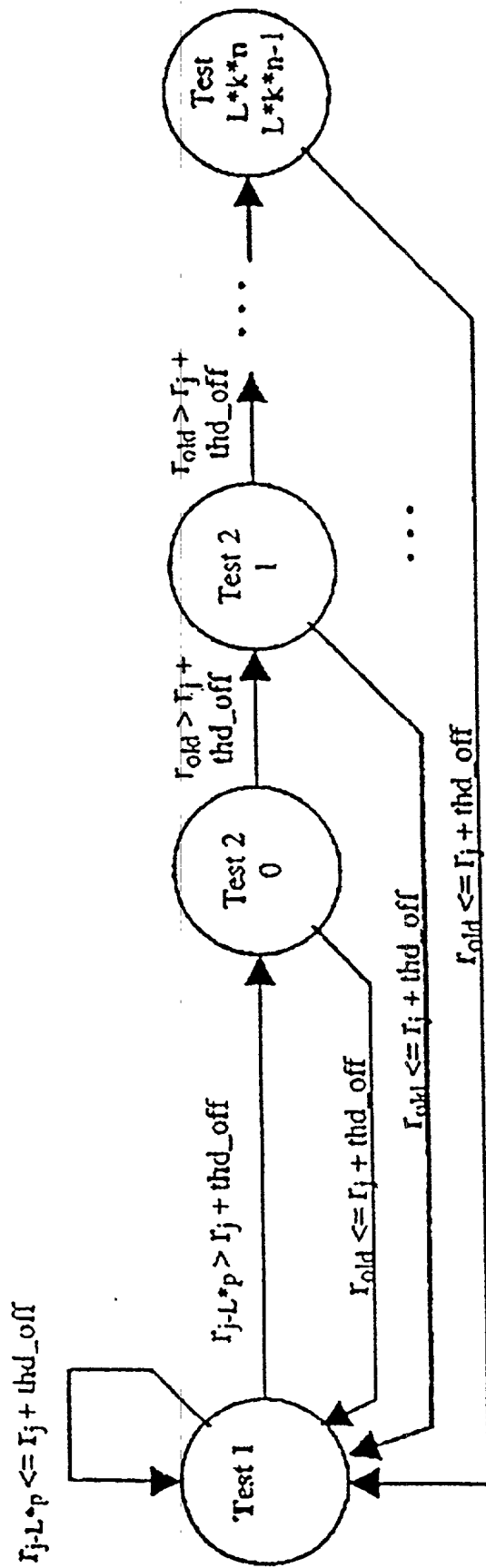


FIG. 61

Table Index	Table Value (dB)
0	0.00
1	3.00
2	6.00
3	9.00
4	12.00
5	15.00
6	18.00
7	21.00
8	24.00
9	27.00
10	30.00
11	33.00
12	36.00
13	39.25
14	42.25
15	45.25
16	48.25
17	51.25
18	54.25
19	57.25
20	60.25
21	63.25
22	66.25
23	69.25
24	72.25
25	75.25
26	78.25
27	81.25
28	84.25
29	87.25
30	90.25
31	93.25

FIG. 62a

Table Index	Table Value (dB)
0	0.00
1	0.25
2	0.25
3	0.50
4	0.50
5	0.75
6	0.75
7	0.75
8	1.00
9	1.00
10	1.25
11	1.25
12	1.50
13	1.50
14	1.50
15	1.75
16	1.75
17	1.75
18	2.00
19	2.00
20	2.00
21	2.25
22	2.25
23	2.25
24	2.50
25	2.50
26	2.50
27	2.75
28	2.75
29	2.75
30	2.75
31	3.00

FIG. 626

FIG. 63a

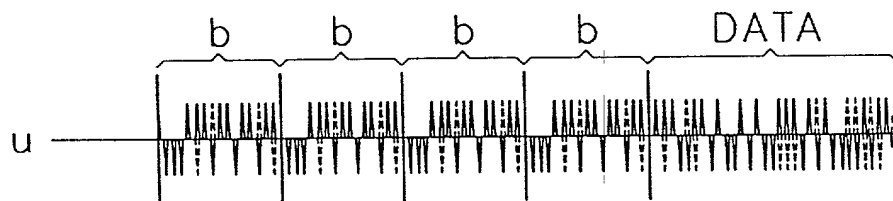
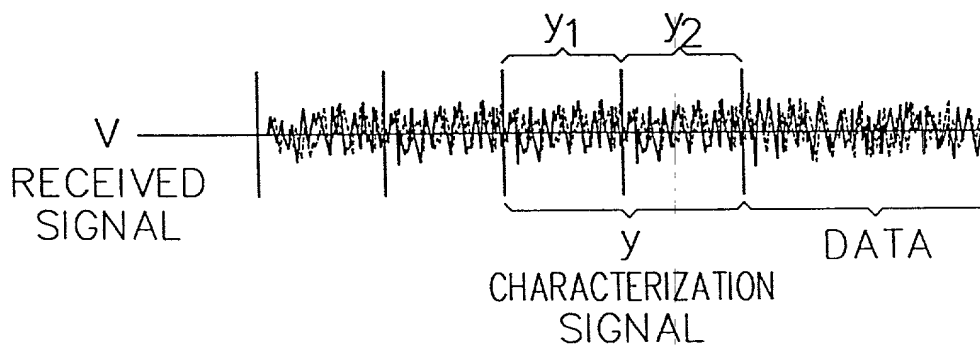


FIG. 63b



FIG. 63c



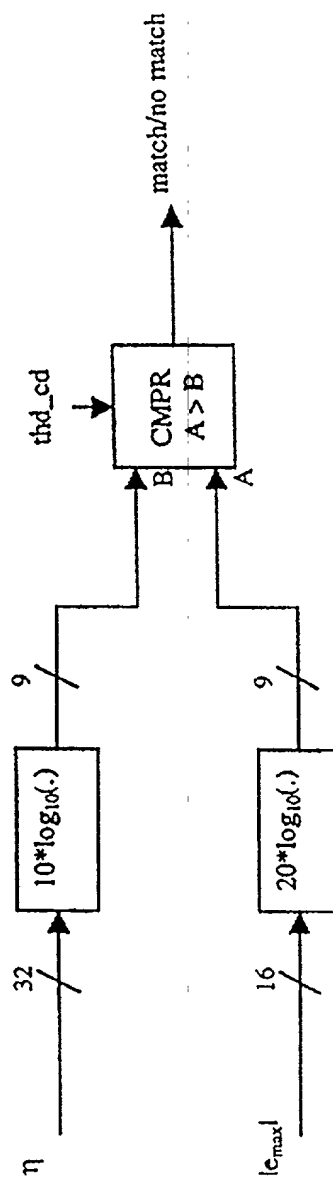
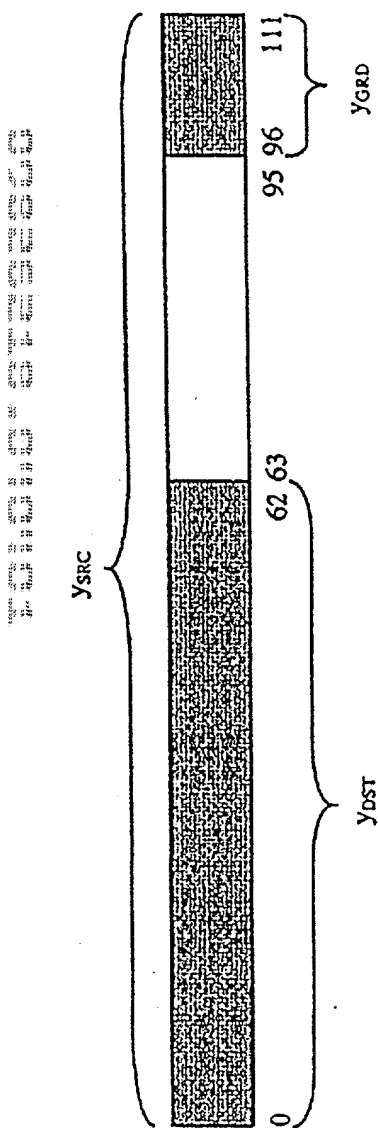
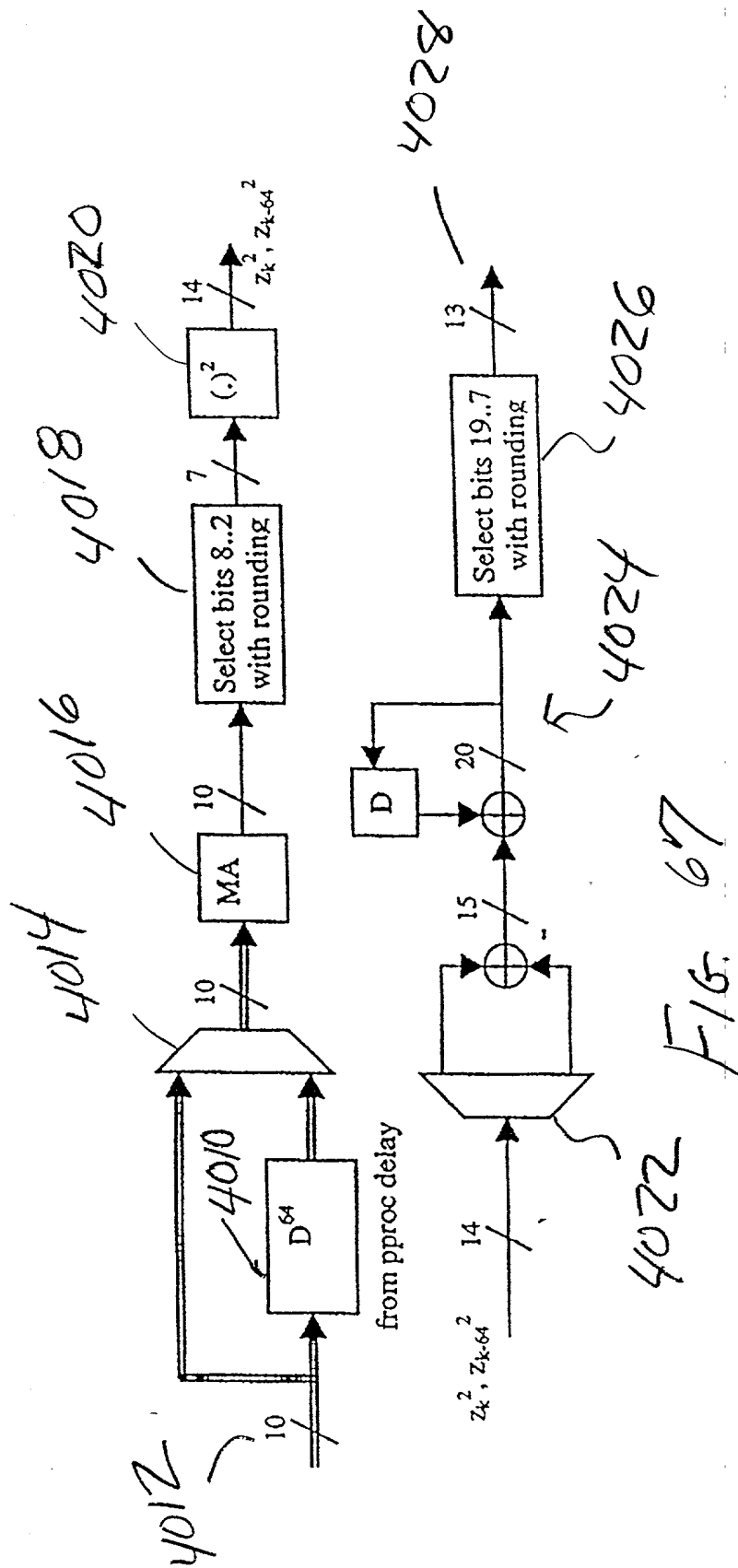


Table Index	Table Value
0	0.00
1	6.00
2	12.00
3	18.00
4	24.00
5	30.00
6	36.00
7	42.25
8	48.25
9	54.25
10	60.25
11	66.25
12	72.25
13	78.25
14	84.25
15	90.25

FIG. 66a

Table Index	Table Value
0	0.00
1	0.50
2	1.00
3	1.50
4	2.00
5	2.25
6	2.75
7	3.25
8	3.50
9	4.00
10	4.25
11	4.50
12	4.75
13	5.25
14	5.50
15	5.75

FIG. 66b



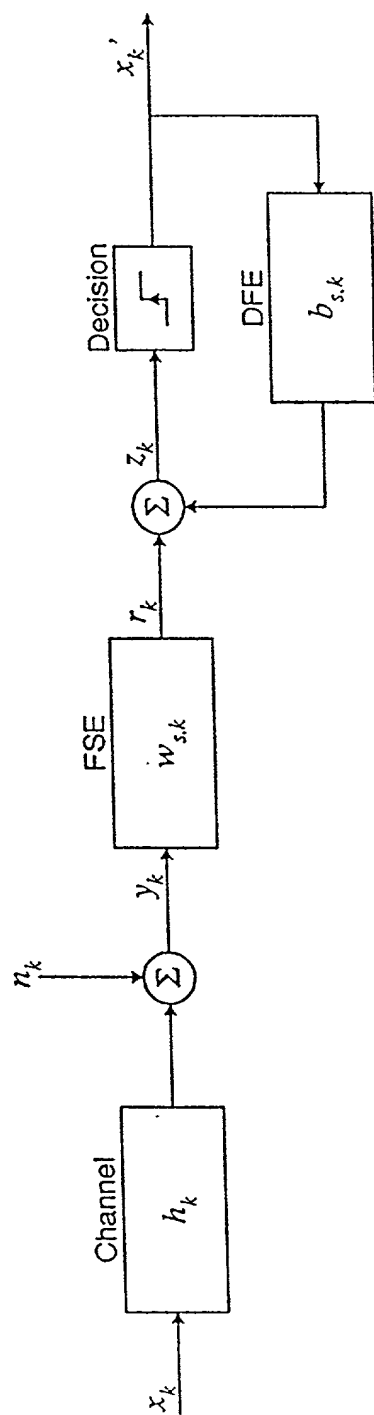


FIG. 68

FIG. 69 is a schematic diagram of a filter and protection component in accordance with the present invention. The component is shown in a perspective view, with a top surface 445, a bottom surface 451, and side surfaces 453 and 459. The component is divided into two main sections, TX (Transmit) and RX (Receive), by a vertical partition 455. The TX section contains a transformer 461a with a primary winding 461b and a secondary winding 461c. The RX section contains a transformer 461b with a primary winding 461d and a secondary winding 461e. The primary windings 461b and 461d are connected to a common input line 445, and the secondary windings 461c and 461e are connected to a common output line 451. The output line 451 is connected to a TIP and RING line 459. The component is also connected to a TRANSMIT line 495 and a RECEIVE line 495. The TRANSMIT line 495 is connected to the TX section, and the RECEIVE line 495 is connected to the RX section. The component is shown in a perspective view, with a top surface 445, a bottom surface 451, and side surfaces 453 and 459. The component is divided into two main sections, TX (Transmit) and RX (Receive), by a vertical partition 455. The TX section contains a transformer 461a with a primary winding 461b and a secondary winding 461c. The RX section contains a transformer 461b with a primary winding 461d and a secondary winding 461e. The primary windings 461b and 461d are connected to a common input line 445, and the secondary windings 461c and 461e are connected to a common output line 451. The output line 451 is connected to a TIP and RING line 459. The component is also connected to a TRANSMIT line 495 and a RECEIVE line 495. The TRANSMIT line 495 is connected to the TX section, and the RECEIVE line 495 is connected to the RX section.

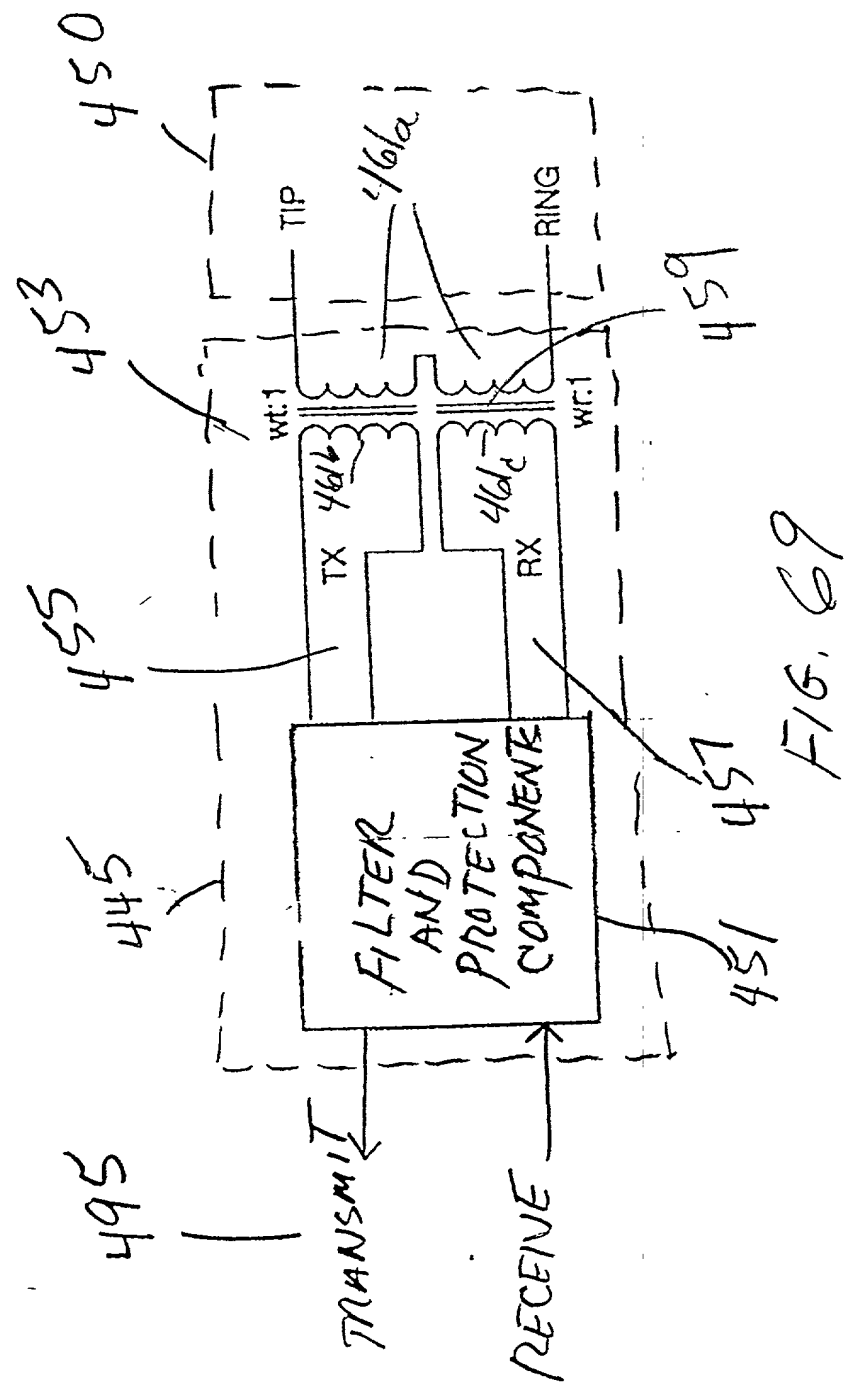
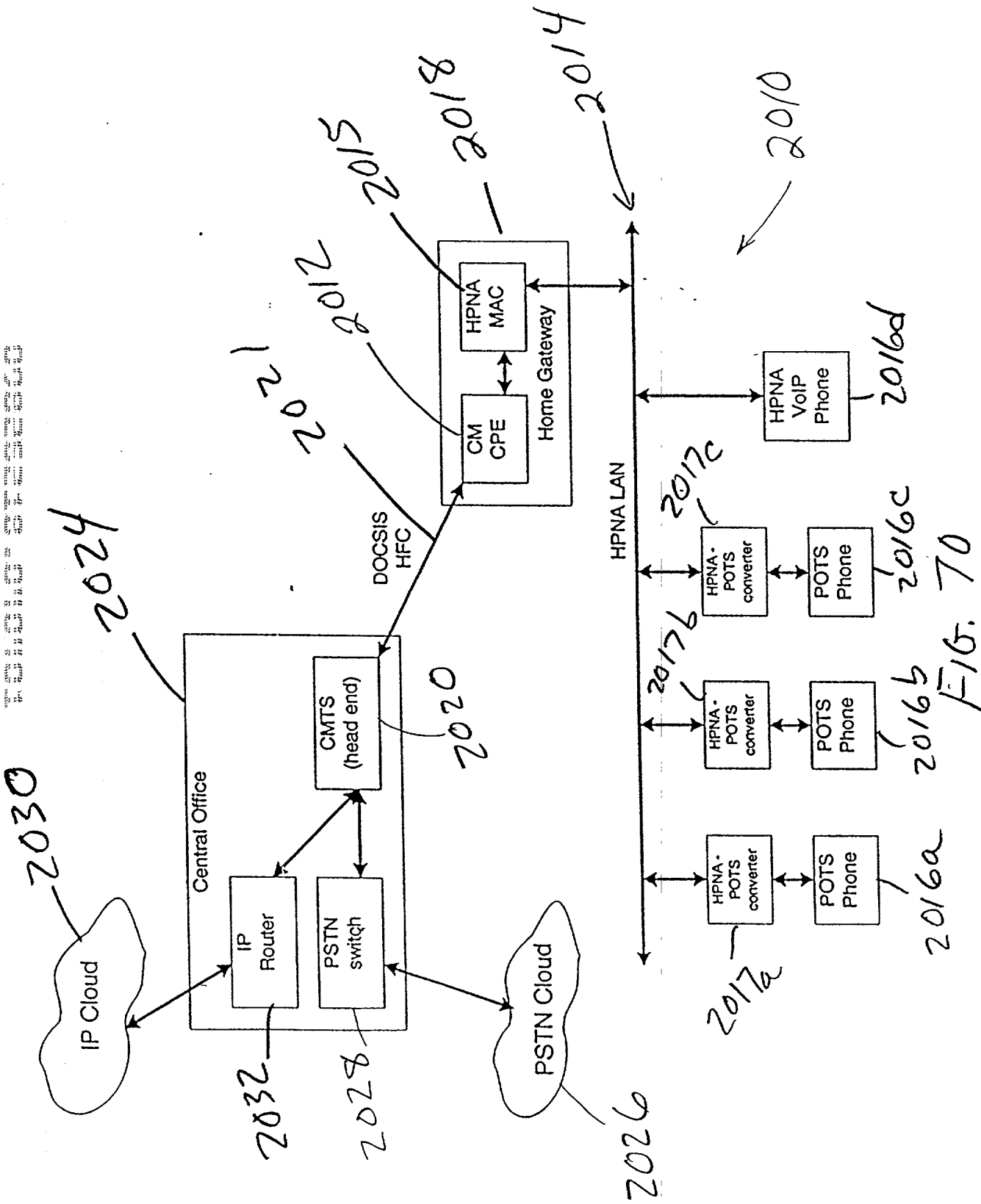


FIG. 69



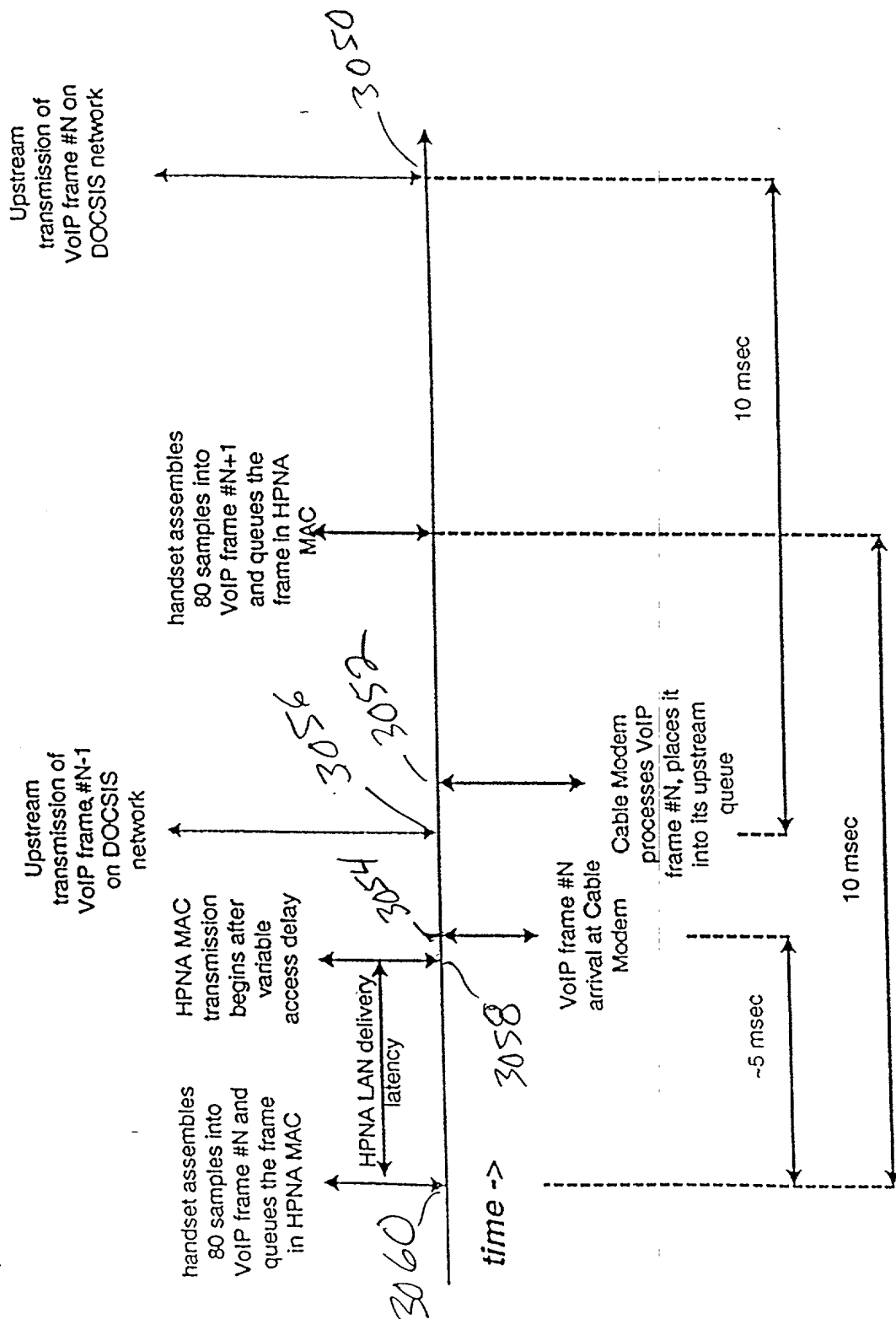


Fig. 71

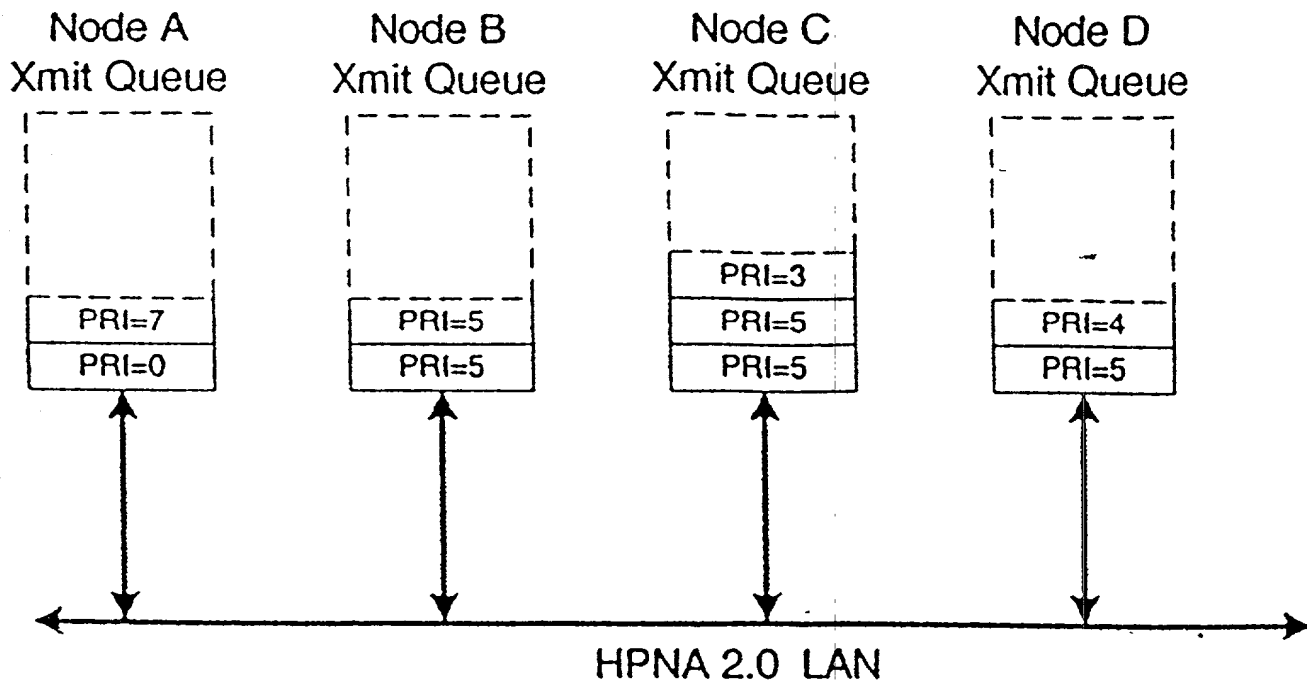


FIG. 72a

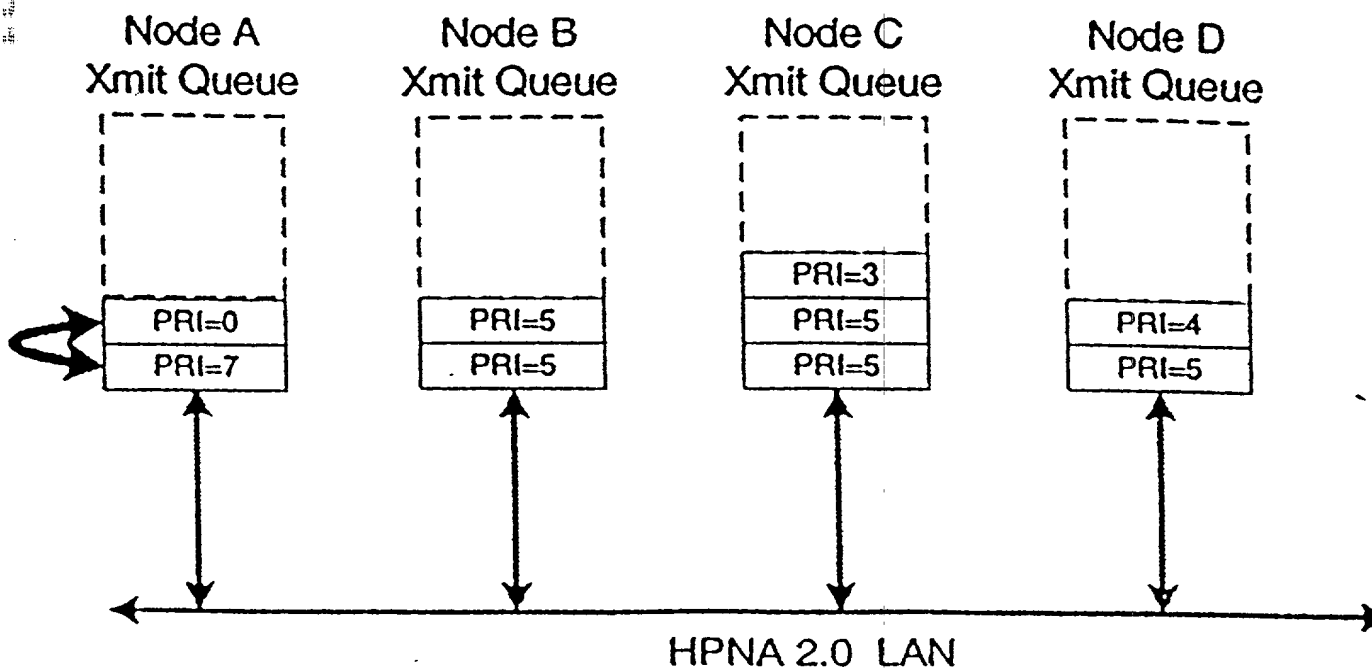


FIG. 72b

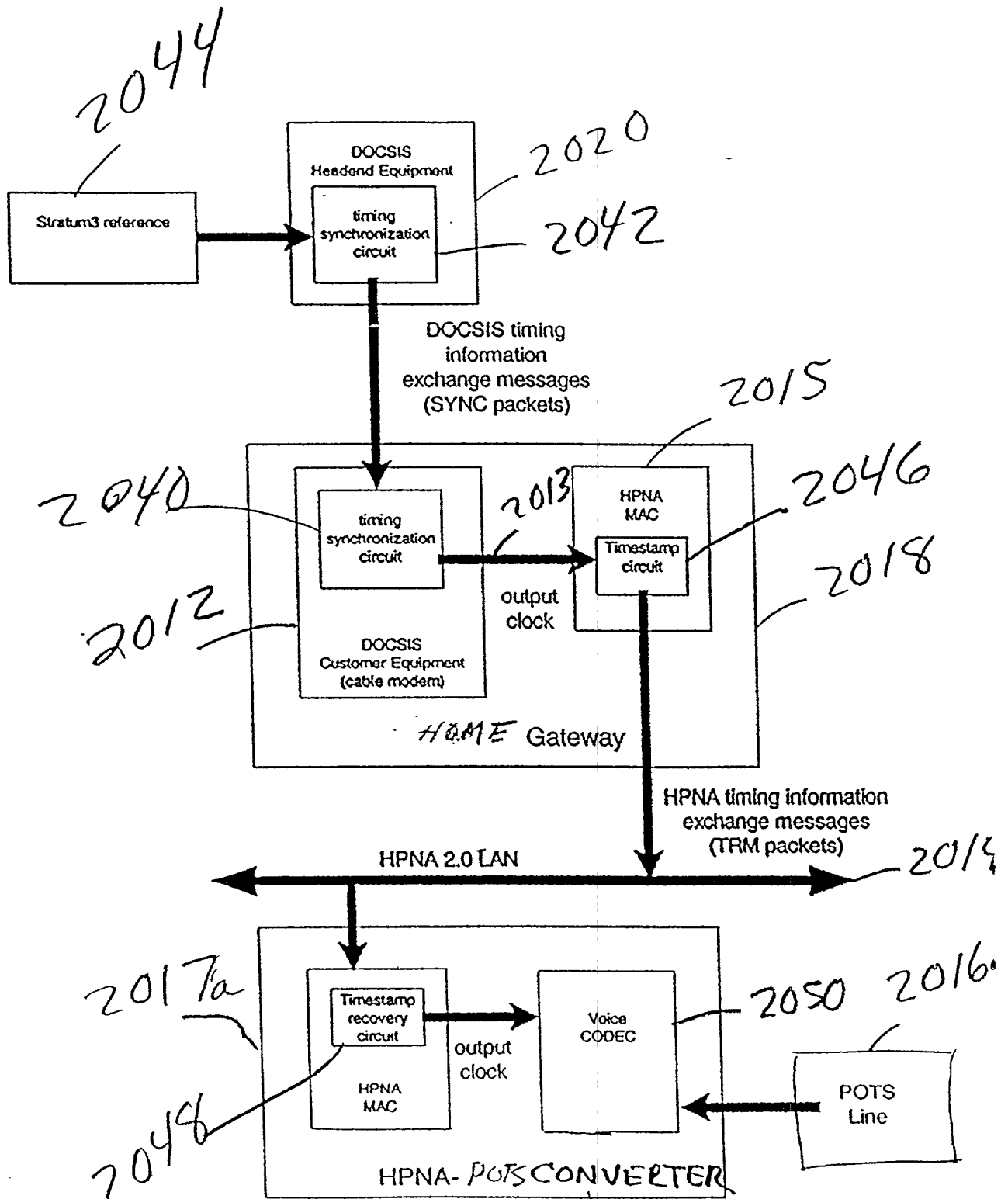


FIG. 73

parameter	UPSTREAM			DOWNSTREAM		
	"10E-6 Case	91% Case	90% Case	"10E-6 Case	91% Case	90% Case
Access delay	3.1	1.3	1.3	3.1	1.3	1.3
Collision Resolution	2.7	2.7	0.8	2.7	2.7	0.8
3 up, 1 down	2.1	1.0	1.0	2.1	1.0	1.0
last up	0.5	0.3	0.3	0.5	0.3	0.3
Collision Resolution	0.8	0.8	0.8	0.8	0.8	0.8
3 up, 1 down	2.1	1.0	1.0	2.1	1.0	1.0
last up	0.5	0.3	0.3	0.5	0.3	0.3
3 down				1.5	0.8	0.8
3 down				1.5	0.8	0.8
Total latency	11.8	7.4	5.5	14.9	8.9	7.1

10E-6 case is 10E-6 CRA once of two tries in homes with maximum 4Mbits/sec raw rate  
 91% case is 10E-6 CRA once of two tries in homes with minimum 10Mbits/sec raw rate  
 90% case is 10E-1 CRA twice in two tries in homes with minimum 10Mbits/sec raw rate

Values in the table above are in milliseconds.

Overheads:					linear PCM	5 nodes	5 nodes	5 nodes
ifg	per coll	frame hdr	Larq hdr	rtp_hdr	frame size	CRA 10E-6	CRA 10E-1	CRA fixed
0.0	0.206	0.07	8	40	160	13	4	2
18								
msec	msec	msec	Bytes	bytes	bytes	collisions	collisions	collisions

Frame header includes preamble, FC, DA, SA, T/L, EOF

FIG. 74

parameter	UPSTREAM			DOWNSTREAM		
	"10E- 6 Case	91% Case	90% Case	"10E- 6 Case	91% Case	90% Case
Access delay	3.1	1.3	1.3	3.1	1.3	1.3
Collision Resolution	0.4	0.4	0.4	0.4	0.4	0.4
3 up, 1 down	1.4	0.8	0.8	1.4	0.8	0.8
last up	0.5	0.3	0.3	0.5	0.3	0.3
Collision Resolution	0.0	0.0	0.0	0.0	0.0	0.0
3 up, 1 down	0.0	0.0	0.0	0.0	0.0	0.0
last up	0.0	0.0	0.0	0.0	0.0	0.0
3 down				1.1	0.6	0.6
3 down				0.0	0.0	0.0
Total latency	5.5	2.7	2.7	6.5	3.3	3.3

FIG. 75

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
DA	6 octets	Destination Address
SA	6 octets	Source Address
Ethertype	2 octets	(TBD) = VOHN Link Control Frame - new IEEE assignment
Type	2 octets	1 = Timestamp Sync Message
Length	2 octets	= 4
Version	2 octets	= 0
SeqNum	2 octets	Timestamp Sync Message Sequence Number
Pad		Any value octet
FCS	4 octets	Frame Check Sequence

FIG. 76

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
DA	6 octet s	Destination Address
SA	6 octet s	Source Address
Ethertype	2 octet s	(TBD) = Vohn Link Control Frame - new IEEE assignment
Type	2 octet s	2 = Timestamp Report Message
Length	2 octet s	Number of additional octets in the signaling frame, starting with Version field and ending with the last octet of the Data Payload field. Minimum is 2.
Version	2 octet s	= 0
TSMSeqNum	2 octet s	Sequence number of TSM to which the Timestamp in this message is applicable.
Timestamp	4 octet s	Timestamp of a previously transmitted Timestamp Report Message, corresponding to TSMSeqNum.
Frequency	2 octet s	Resolution of the timestamp and Gtimestamp fields, in ticks/1.000ms. For example, value 32768 corresponds to one clock tick at 32.768Mhz, in which the LSBit of the Timestamp corresponds to a time of 0.030517578125usec. The Timestamp will rollover every 131 seconds = 2.2 minutes
NumGrants	2 octet s	Number of Grant Timestamps specified in the payload of this control message. NumGrants may be zero. Each grant timestamp is accompanied by a Line ID and Call ID field. Including the Grant Timestamp, the total for each grant timestamp is 8 bytes.

FIG. 77(1)

Line ID	2 octet s	Identifier of the Line termination associated with the immediately following GTimestamp.
Call ID	2 octet s	Identifier of the call instance on the Line termination associated with the immediately following GTimestamp.
GrantTimestamp	4 octet s	Grant Timestamp corresponding to the immediately preceding Line ID. This is the time at which the Proxy Gateway wishes to receive a future constant bit rate service flow packet in order to minimize delivery latency to subsequent delivery to a synchronous network. The time value corresponds to the time at the timing master. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time.
...		additional instances of {Line ID, Call ID, Grant Timestamp} field tuples
Pad		Any value octet
FCS	4 octet s	Frame Check Sequence

Fig. 77(2)

PIN NAME	CM-side Function (HPNA timing master)		Handset Function (HPNA timing slave)	
DPLL_REF_CLK	DPLL input clock	IN		
Grant[4]	Grant Present Indication	IN		
Grant[3]	Grant SID Value[3]	IN		
Grant[2]	Grant SID Value[2]	IN		
Grant[1]	Grant SID Value[1]	IN		
Grant[0]	Grant SID Value[0]	IN		
V_CLK_OUT			DPLL output clock	OUT
GPI[0]			Grant Present Indication[0]	OUT
GPI[1]			Grant Present Indication[1]	OUT

F16. 78

PIN NAME	CM-side Function (HPNA timing master)		Handset Function (HPNA timing slave)	
DPLL_REF_CLK	DPLL input clock	IN		
Grant[4]	Grant Present Indication	IN		
Grant[3]	Grant SID Value[3]	IN		
Grant[2]	Grant SID Value[2]	IN		
Grant[1]	Grant SID Value[1]	IN		
Grant[0]	Grant SID Value[0]	IN		
V_CLK_OUT			DPLL output clock	OUT
Frame[0]			Frame boundary marker[0]	OUT
Frame[1]			Frame boundary marker[1]	OUT

Fig. 79

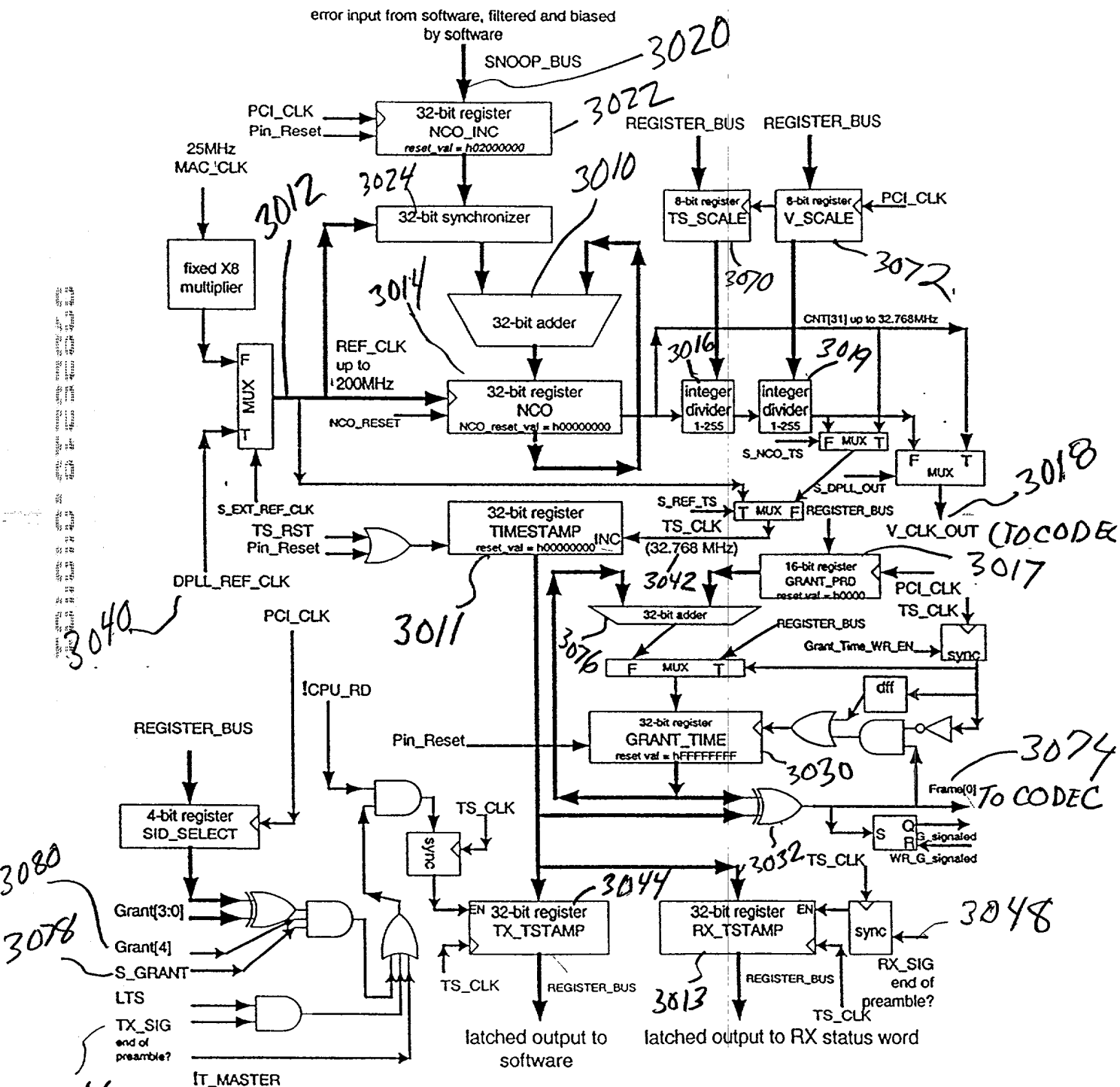


FIG. 80

Output jitter, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000

200MHz to 32.768MHz

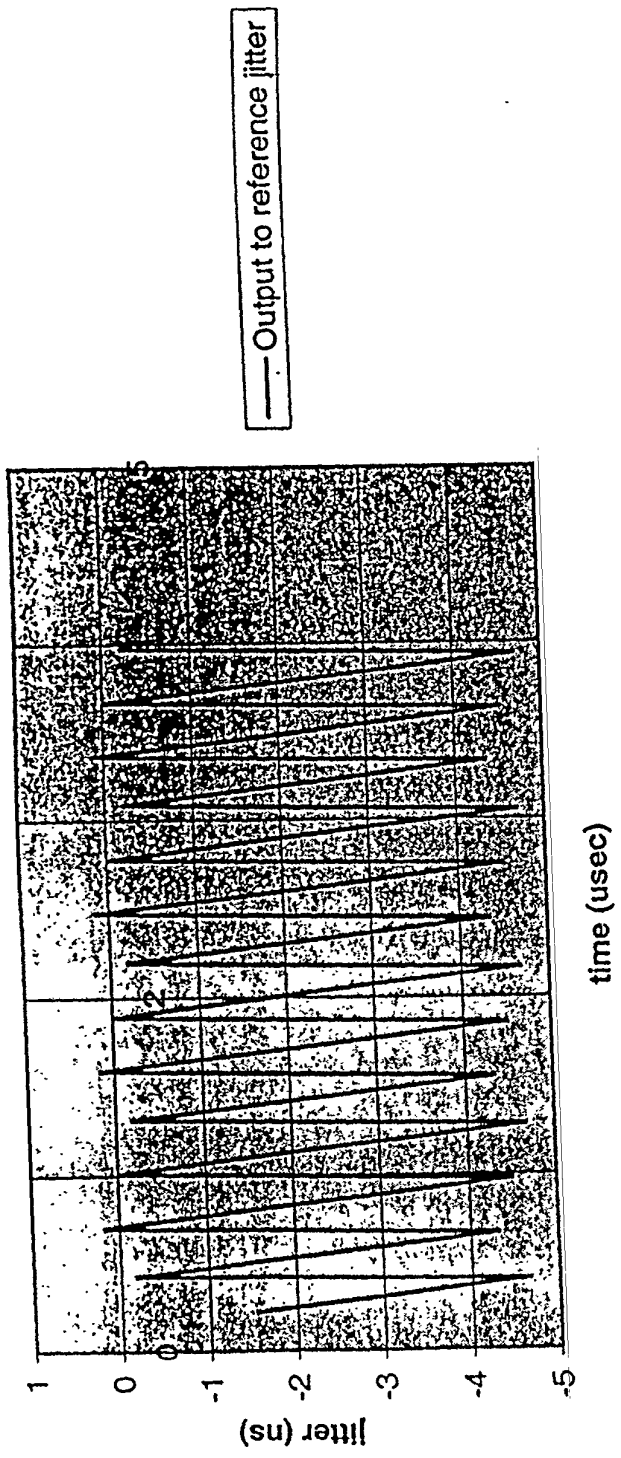


FIG. 81

FIG. 82 is a block diagram of a system for generating a timestamp and outputting it to a register bus. The system includes a 32-bit register (TIMESTAMP) with a reset value of 00000000. The register is clocked by TS\_CLK (32.768MHz) and reset by TS\_RST and Pin\_Reset. The output of the register is connected to a 4-bit register (SID\_SELECT) and a 32-bit register (TX\_TSTAMP). The 4-bit register is clocked by PCI\_CLK and its output is connected to the 32-bit register (TX\_TSTAMP). The 32-bit register (TX\_TSTAMP) is clocked by TS\_CLK and its output is connected to the REGISTER\_BUS. The REGISTER\_BUS is also connected to a 32-bit register (RX\_TSTAMP) and a 32-bit register (EN 32-bit register TX\_TSTAMP). The 32-bit register (RX\_TSTAMP) is clocked by TS\_CLK and its output is connected to the REGISTER\_BUS. The 32-bit register (EN 32-bit register TX\_TSTAMP) is clocked by TS\_CLK and its output is connected to the REGISTER\_BUS. The REGISTER\_BUS is also connected to a 32-bit register (RX\_TSTAMP) and a 32-bit register (EN 32-bit register TX\_TSTAMP). The 32-bit register (RX\_TSTAMP) is clocked by TS\_CLK and its output is connected to the REGISTER\_BUS. The 32-bit register (EN 32-bit register TX\_TSTAMP) is clocked by TS\_CLK and its output is connected to the REGISTER\_BUS.

DPLL\_REF\_CLK

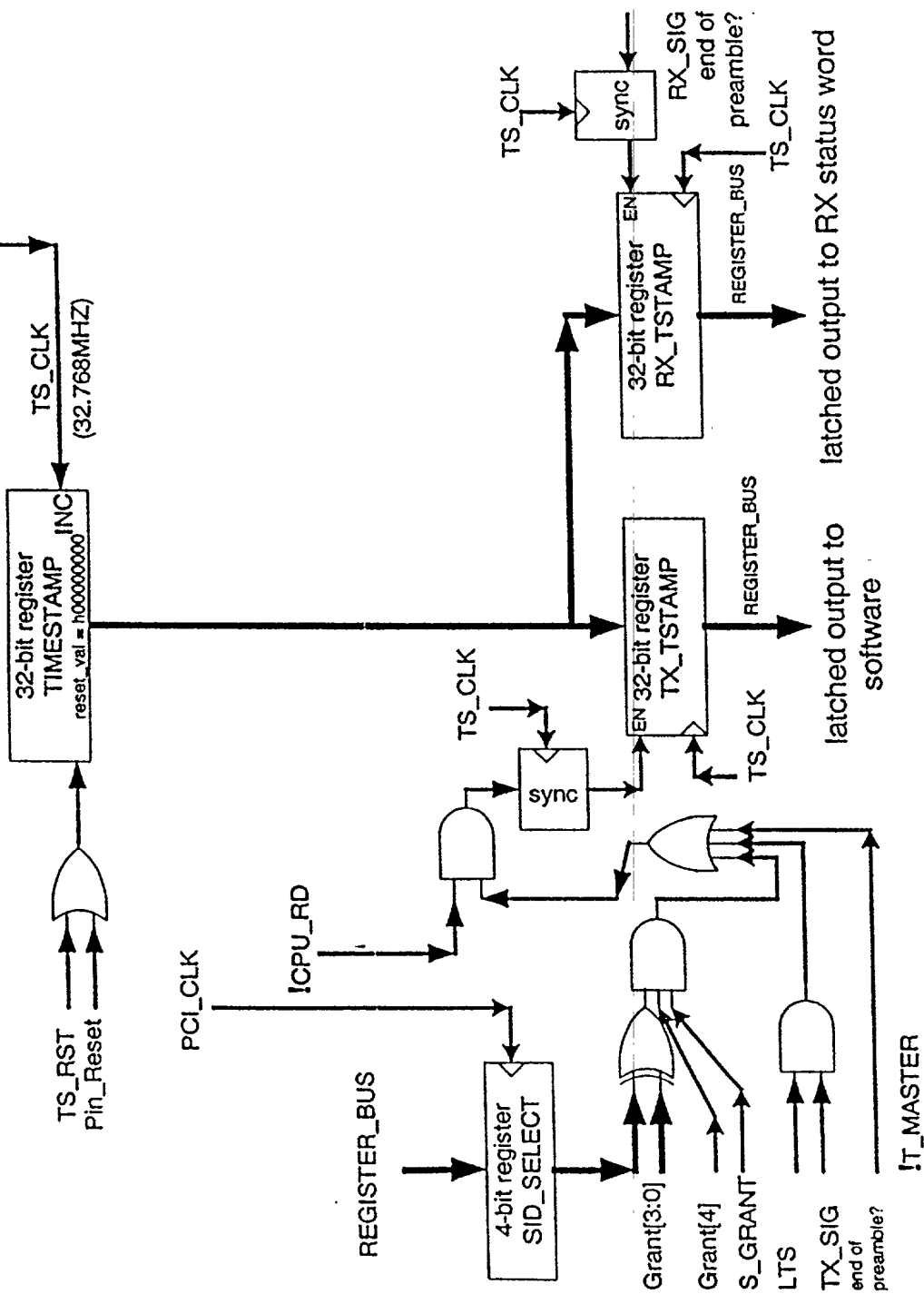


FIG. 82

PIN NAME	CM-side Function (HPNA timing master)		Handset Function (HPNA timing slave)	
DPLL_REF_CLK	Timestamp input clock	IN	Timestamp input clock	
Grant[4]	Grant Present Indication	IN	NA	
Grant[3]	Grant SID Value[3]	IN	NA	
Grant[2]	Grant SID Value[2]	IN	NA	
Grant[1]	Grant SID Value[1]	IN	NA	
Grant[0]	Grant SID Value[0]	IN	NA	

FIG. 83a

Bit locations	Field name	Description
7-3	Reserved	
2	TsReset	When set to 1, forces timestamp register to value of 0x00000000. When set to 0, allows timestamp register to increment by one for each detected DPLL_REF_CLK rising edge.
1	SGrant	When set to 1, causes timestamp to be latched into txTimeStampHigh and txTimeStampLow registers whenever the value of tscSID matches the value of input pins Grant[3:0] and Grant[4] is asserted. When set to 0, disables txTimeStampHigh and txTimeStampLow latching under the stated conditions.
0	TMaster	When set to 1, enables txTimeStampHigh and txTimeStampLow registers to be latched with timestamp values at times determined by frame transmissions (through the LTS descriptor bit) or grant events (through the sGrant descriptor bit). When set to 0, enables txTimeStampHigh and txTimeStampLow registers to be latched with timestamp values at times determined by txTimeStampHigh and txTimeStampLow register read accesses.

Default value of this register is 0x05

FIG. 83b

Bit locations	Field name	Description
7-4	Reserved	
3-0	SID	SID value that is to be matched by Grant[3:0] pins in order to cause a grant timestamp value to be latched. When the Grant[3:0] pins match the SID value and the Grant[4] input is 1 and the sGrant register bit is 1, then the current timestamp value will be latched into the txTimeStampHigh and txTimeStampLow registers.

Default value of this register is 0x00

FIG. 83c

Bit locations	Field name	Description
15-0	txTimeStampLow	Least significant 16 bits of the latched tx timestamp value

Default value of this register is undefined.

*Fig. 83d*

Bit locations	Field name	Description
15-0	txTimeStampHigh	Most significant 16 bits of the latched tx timestamp value

Default value of this register is undefined.

*Fig. 83e*

Bit locations	Field name	Description
15-0	rxTimeStampLow	Least significant 16 bits of the latched rx timestamp value

Default value of this register is undefined.

*Fig. 83f*

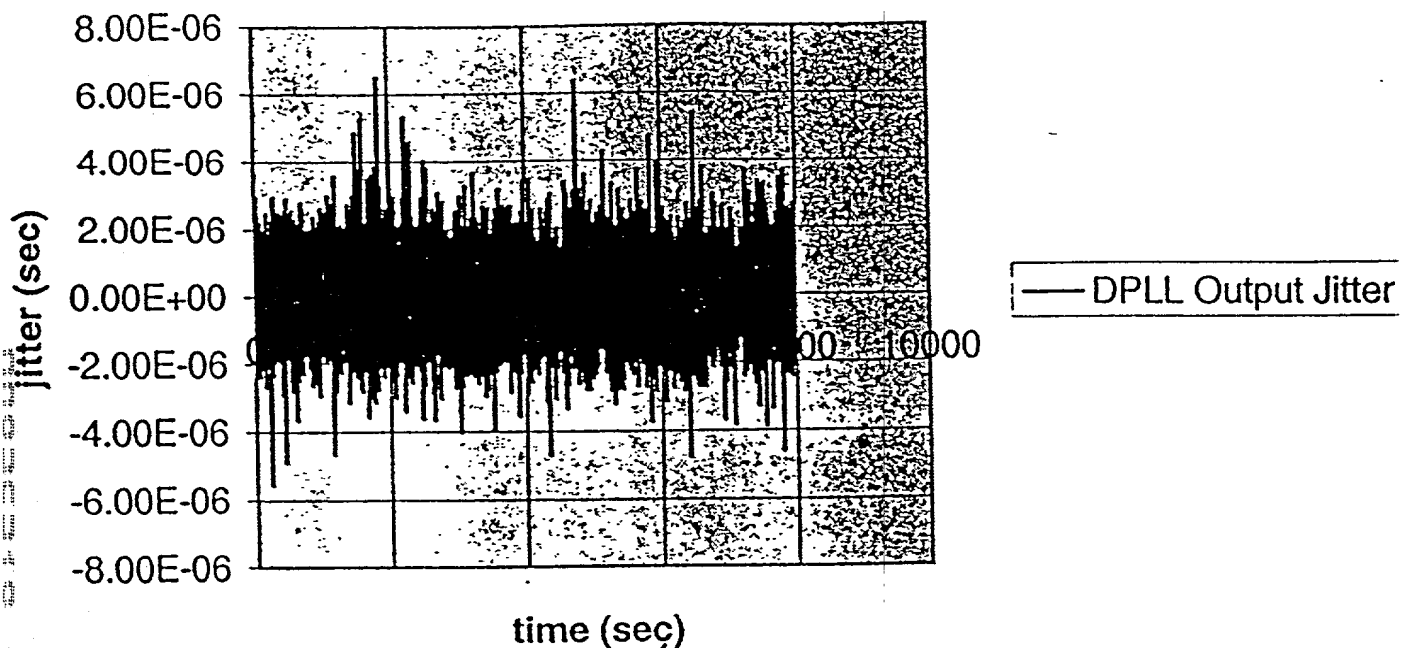
Bit locations	Field name	Description
15-0	rxTimeStampHigh	Most significant 16 bits of the latched rx timestamp value

Default value of this register is undefined.

*Fig. 83g*

# DPLL Output Jitter

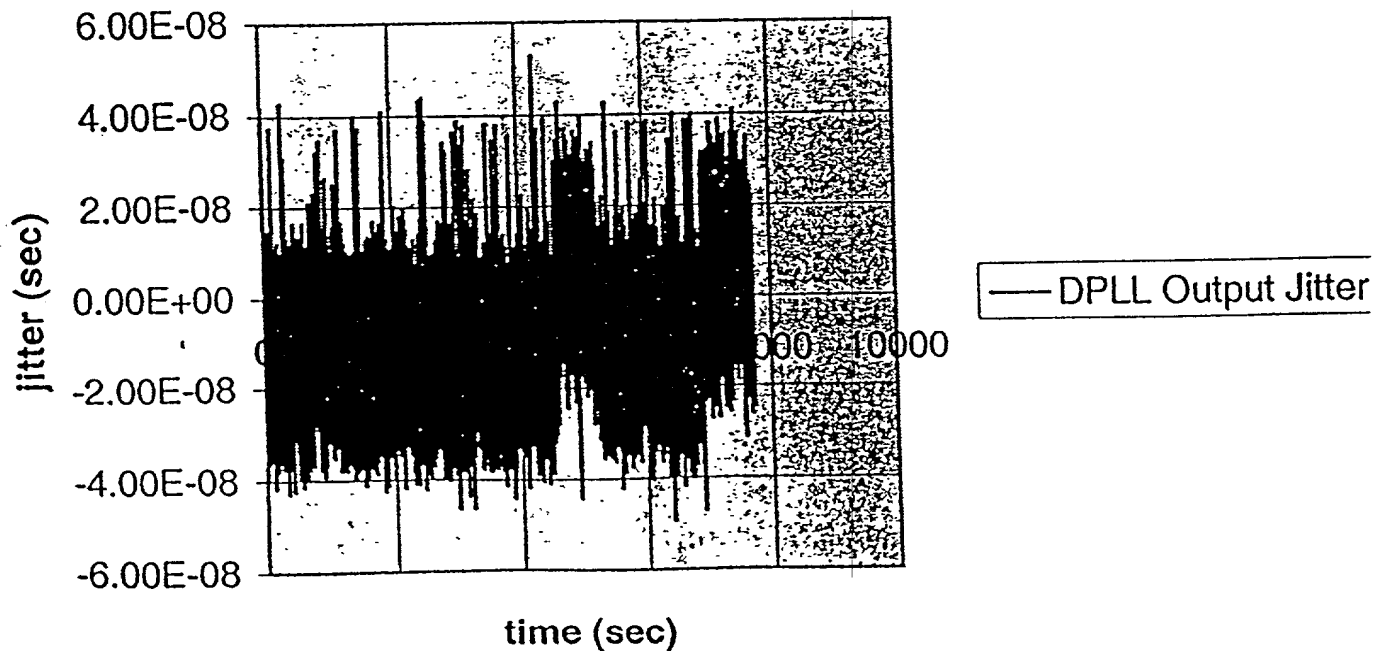
TS=24.576MHz, TRM=1.0sec, lg=0.9, ig=0.1, tgood=0.95,  
m\_j\_dev=1ppm



*Fig. 84a*

# DPLL Output Jitter

TS=24.576MHz, TRM=1.0sec, lg=0.9, ig=0.1, tgood=0.95,  
m\_j\_dev=0ppm



*Fig 84b*

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= TBD
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ethertype field. Minimum is 16.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x00 means that this is a TRM containing a valid timestamp. Value of x01 means that the master does not have a valid clock and slaves should give local indication that they are no longer locked to a master reference. Value of x80 means that this is a TQM. Value of x81 means that this is a TSM. All other values are reserved.
TRMSeqNum	2 octets	Timestamp Report Message Sequence Number for this message. Sequence number of x0000 indicates an initial TRM, implying that Timestamp and PrevTRMSeqNum are both invalid.
PrevTRMSeqNum	2 octets	Sequence number of TRM to which the Timestamp in this message is applicable. The value of PrevTRMSeqNum is not necessarily equal to TRMSeqNum minus one. PrevTRMSeqNum is set to x0000 for the first TRM of a TRM pair.

Fig. 85(1)

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
Timestamp	4 octets	Timestamp of a previously transmitted Timestamp Report Message, corresponding to PrevTRMSeqNum. The LSBit of the Timestamp corresponds to a time of $0.030517578125\mu\text{sec}$ = one clock tick at 32.768MHz. The Timestamp will rollover every 131 seconds = 2.2 minutes.
NumSlots	1 octet	Number of Slot Timestamps specified in the payload of this control message. NumSlots may be zero. Each Slot Timestamp is accompanied by a MACAddr, and Channel_ID field. Including the Slot Timestamp, each Slot Timestamp is 12 bytes long.
PAD_0	3 octets	Padding to align to a 32-bit boundary. Always present, even when NumSlots has the value of 0.
MACAddr	6 octets	MAC Address associated with the immediately following Channel_ID and STimestamp.
Channel_ID	2 octets	Identifier for a channel associated with the immediately preceding MACAddr.
STimestamp	4 octets	Slot Timestamp corresponding to the immediately preceding Channel_ID. This is the time at which the TRM sender wishes to receive a future constant bit rate service flow packet in order to minimize overall latency of delivery to a synchronous network. The time value corresponds to the time at the timing master. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time. The LSBit of the STimestamp corresponds to a time of $0.030517578125\mu\text{sec}$ = one clock tick at 32.768MHz.
MACAddr	6 octets	MAC Address associated with the immediately following Channel-ID and STimestamp.
Channel_ID	2 octets	Identifier for a channel associated with the immediately following Channel_ID and STimestamp.

FIG. 85(2)

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
STimestamp	4 octets	Slot Timestamp corresponding to the immediately preceding Channel_ID. This is the time at which the TRM sender wishes to receive a future constant bit rate service flow packet in order to minimize overall latency of delivery to a synchronous network. Additional packets for the identified service flow are expected to arrive at periodic intervals measured from this time. The LSBit of the STimestamp corresponds to a time of $0.030517578125\mu\text{sec}$ = one clock tick at 32.768 MHz.
...		[additional instances of MACAddr, Channel_ID and Gtimestamp fields, until the number of Gtimestamp fields equals NumGrants]
Next Ethertype	2 octets	= 0
Pad	max (0, 44 - SSLength) octets	Any value octet
FCS	4 octets	

FIG. 85(3)

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= 6
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ether type field. Minimum is 4.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x80 means that this is a TQM.
Next Ether type	2 octets	= 0
Pad	MIN(0,4 0- SSLength) octets	Any value octet
FCS	4 octets	

FIG. 86

<u>Field</u>	<u>Length</u>	<u>Meaning</u>
DA	6 octets	Destination Address (FF.FF.FF.FF.FF.FF)
SA	6 octets	Source Address
Ethertype	2 octets	0x886c (HPNA Link Control Frame)
SSType	1 octet	= 6
SSLength	1 octet	Number of additional octets in the control header, starting with the SSVersion field and ending with the second (last) octet of the Next Ether type field. Minimum is 4.
SSVersion	1 octet	= 0
TRM_type	1 octet	Value of x81 means that this is a TSM.
Next Ether type	2 octets	= 0
Pad	MIN(0, 4 0- SSLengt h) octets	Any value octet
FCS	4 octets	

FIG. 87

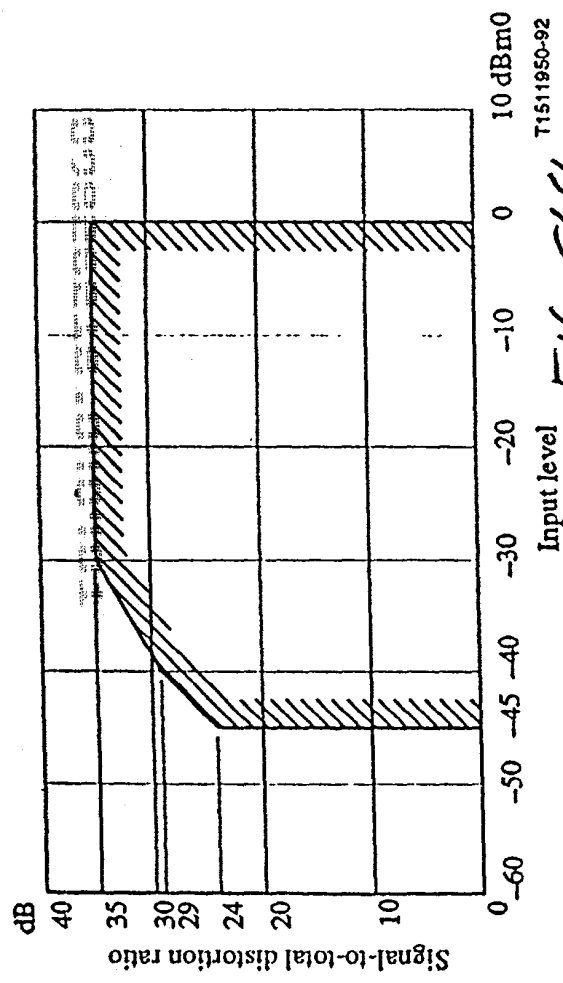


FIG. 88

Input Level	Uniform Quantizer + Compander SNR	The required SNR for the ADC/DAC
0 dBm	38.43 dB	60 dB
-30 dBm	35.50 dB	54 dB
-40 dBm	30.09 dB	44 dB

FIG. 89a

Input Level	G.712 SNR Spec	The total SNR with Uniform Quantizer + Compander + jitter Clock
0 dBm	35 dB	38.32 dB (60 dB ADC/DAC SNR is used)
-30 dBm	35 dB	35.42 dB (54 dB ADC/DAC SNR is used)
-40 dBm	29 dB	30.05 dB (44 dB) ADC/DAC SNR is used)

FIG. 89b

Input Level	G.712 SNR Spec	The total SNR with Uniform Quantizer + Compander + jitter Clock
0 dBm	35 dB	38.38 dB (60 dB ADC/DAC SNR is used)
-30 dBm	35 dB	35.26 dB (54 dB ADC/DAC SNR is used)
-40 dBm	29 dB	30.03 dB (44 dB) ADC/DAC SNR is used)

FIG 89c

Figure 90: A graph showing the jitter time waveform. The y-axis is labeled "Amplitude in ns" and ranges from -3 to 3. The x-axis is labeled "Time in us" and ranges from 0 to 35. The waveform is a periodic sawtooth pattern with a period of approximately 10 us. The amplitude of the peaks is approximately 2.5 ns, and the amplitude of the troughs is approximately -2.5 ns.

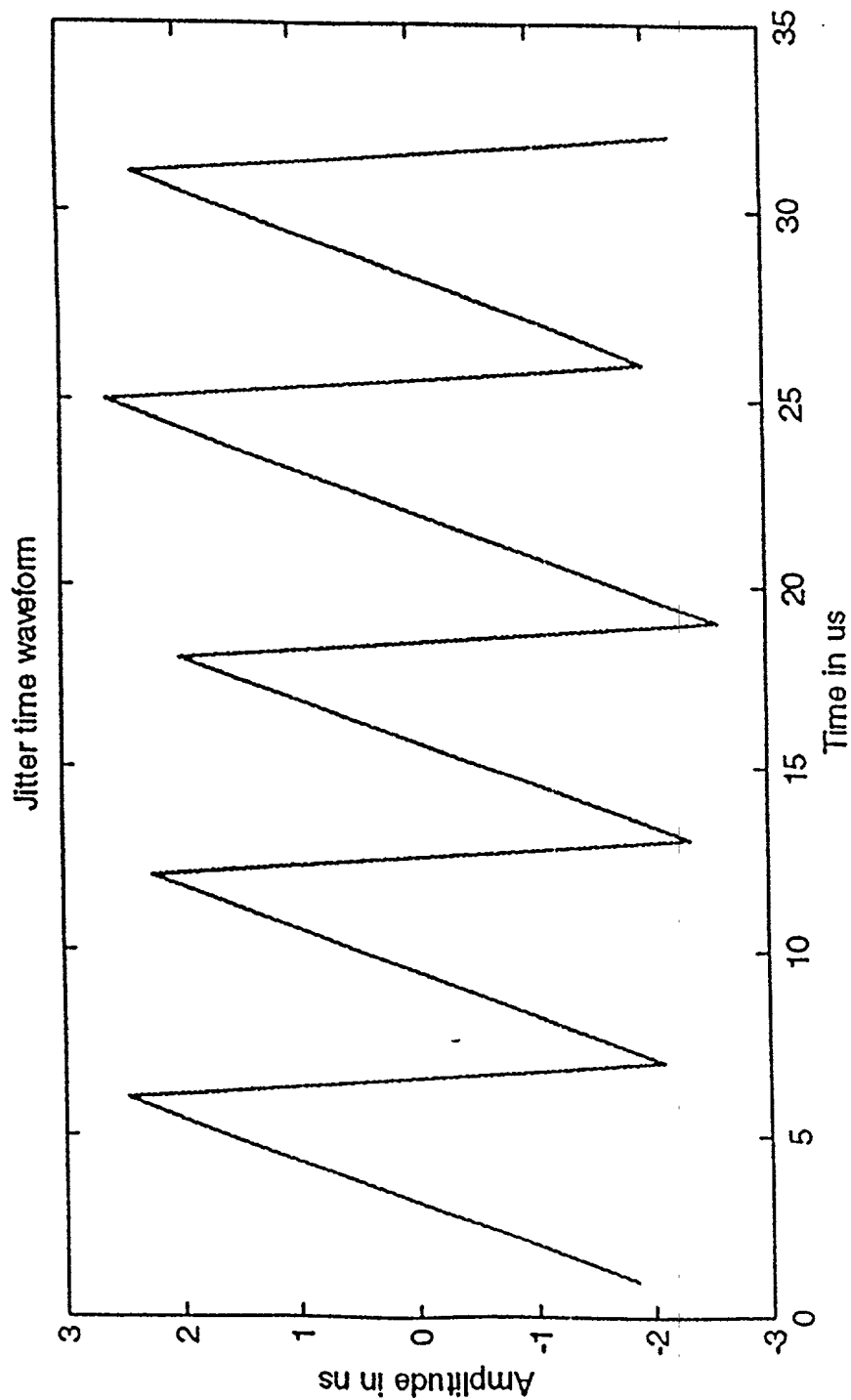


FIG. 90

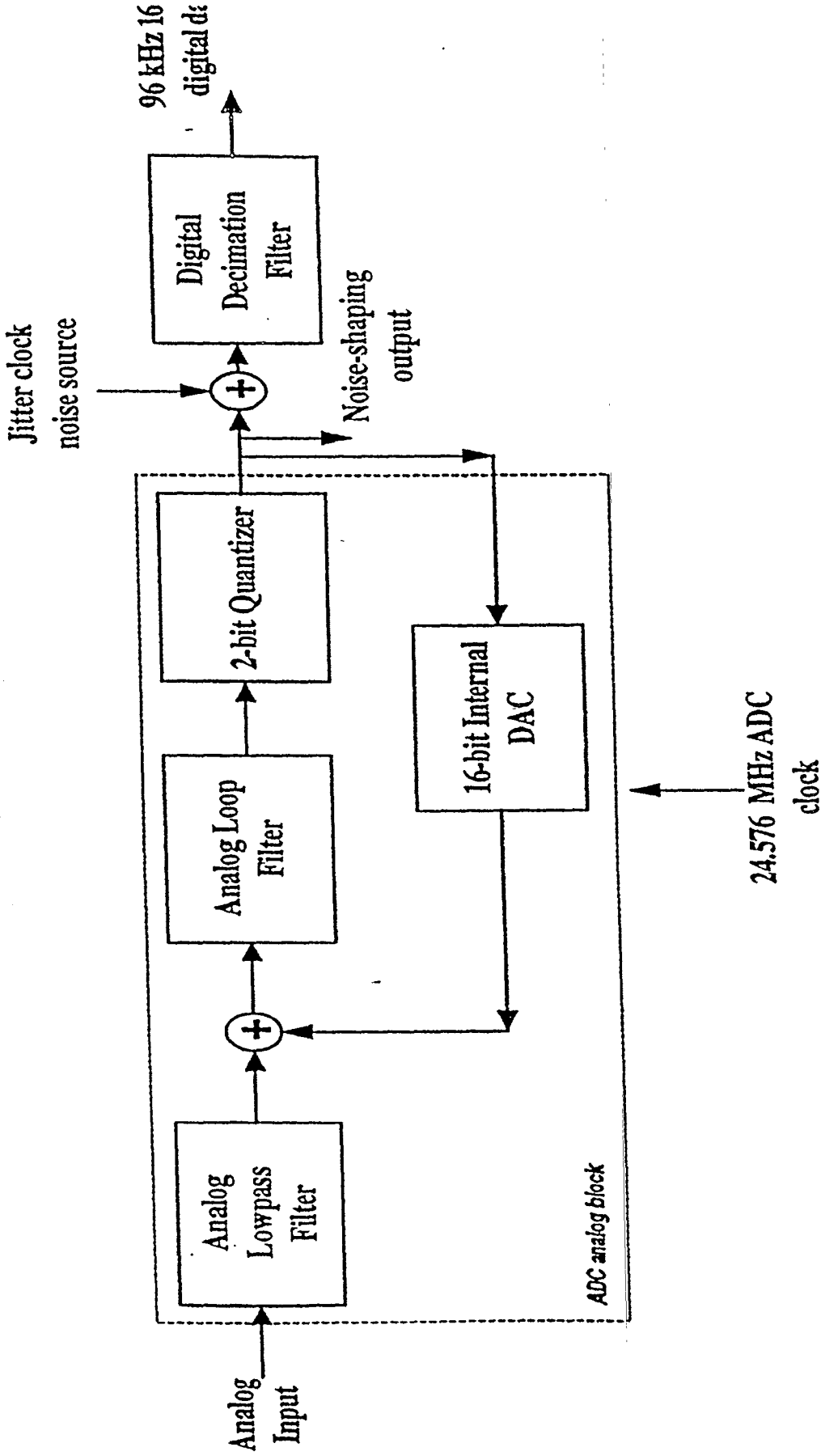


FIG. 91



Octet	Field	Length	Description
Flags 0	TxPriority7	1	Station is (was) transmitting frames with LL priority 7. (always set)
	TxPriority6	1	Station is (was) transmitting frames with LL priority 6.
	TxPriority5	1	Station is (was) transmitting frames with LL priority 5.
	TxPriority4	1	Station is (was) transmitting frames with LL priority 4.
	TxPriority3	1	Station is (was) transmitting frames with LL priority 3.
	TxPriority2	1	Station is (was) transmitting frames with LL priority 2.
	TxPriority1	1	Station is (was) transmitting frames with LL priority 1.
	TxPriority0	1	Station is (was) transmitting frames with LL priority 0. (always set)
Flags 1	Reserved	5	Shall be sent as 0 and ignored by 2.0 stations when received.
	CSS_Master_Capability	1	This station is capable of operating as a CSS Master node.
	No_V1M2_Frames	1	This station does not support the reception or transmission of compatibility frames (V1M2 frames).
	Supports 4Mbaud	1	This station supports 4 megabaud payload encodings.
Flags 2	Reserved	8	Shall be sent as 0 and ignored by 2.0 stations when received.
Flags 3	ConfigV2	1	Force use of 10M8 mode, defers to Config1 and ConfigV1Ms.
	ConfigV1M2	1	Force use of HPNA V1M2 mixed mode, defers to ConfigV1.

FIG. 93(1)

Octet	Field	Length	Description
	ConfigV1	1	Force use of HPNA 1.x mode, highest precedence of config flags.
	Reserved	2	Shall be sent as 0 and ignored by 2.0 stations when received.
	Highest Version	3	This station's highest supported HPNA version: 0x000 -- Reserved 0x001 -- HPNA 1.0 0x010 -- HPNA 2.0 0x001-0x111 Reserved

F16.93(2)

<u>Field</u>	<u>Length</u> <u>h</u>	<u>Meaning</u>
CSEType	1 octet	X00 = signifies a CSS Extension type
CSELength	1 octet	X08 = Number of additional octets in this CSEType. CSELength is always x08 for CSEType = x00 = CSS
CSS_MAC	6 octets	MAC address of client station
CSS_SEQ	2 octets	<p>CSS sequence, 8 two-bit values concatenated: 0-2 indicate a specific signaling slot, while 3 indicates the use of a randomly selected value chosen by the client at the time of the collision.</p> <p>X0000 - xBFFF = assigned CSS_SEQ value for the node possessing the MAC address specified in CSS_MAC</p> <p>XC000 - xFEFF = reserved</p> <p>XFF00 = indication by the client node specified by CSS_MAC that it is no longer an active sender of link layer priority 6 frames (equivalent to a "0 active channels" indication)</p> <p>XFF01 - xFFFE = request by the client node specified by CSS_MAC for a CSS Sequence from the master node. The 8 Least significant bits indicate the number of active channels which are sending link layer.</p> <p>priority 6 frames for this client.</p> <p>XFFFF - reserved</p>

FIG. 94

2-bit CSS register value (binary)	Signal slot integer (decimal)
00	0
01	1
10	2
11	Random in range [0,2]

FIG. 95

FIG. 95 is a table showing the mapping of 2-bit CSS register values to signal slot integers. The table has two columns: '2-bit CSS register value (binary)' and 'Signal slot integer (decimal)'. The rows are: 00 maps to 0, 01 maps to 1, 10 maps to 2, and 11 maps to 'Random in range [0,2]'.

Bit Number	Value
7:0	<b>Station Type:</b> 0 – HomePNA 1.x station 1 – 10M8 station in V1M2 Mode 2 – 10M8 station in V1M2 Mode, that has detected a recent 1M8 transmission with PCOM Station Type = 0 Other values reserved
31:8	Reserved, must be 0 on transmission

*FIG. 96*

Precedence	Variable
1	ConfigV1
2	ConfigV1M2
3	ConfigV2
4	V1_DETECTED
4	V1_SIGNALED

*FIG. 97*

UNITED STATES PATENT AND TRADEMARK OFFICE  
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# Oath/Declaration, Small Entity, and Power of Attorney

8

Level - 2  
Version 1.1

DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION

PATENT

Docket No. : 42141/RJP/E264

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A METHOD FOR PROVIDING DYNAMIC ADJUSTMENT OF FRAME ENCODING PARAMETERS IN A FRAME-BASED COMMUNICATIONS NETWORK, the specification of which is attached hereto unless the following is checked:

\_\_\_ was filed on \_\_\_ as United States Application Number or PCT International Application Number \_\_\_ and was amended on \_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of the foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below, any foreign application for patent or inventor's certificate, or any PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)Application Number CountryFiling Date (day/month/year) Priority Claimed

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number Filing Date

60/196,002 April 7, 2000

60/197,224 April 14, 2000

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112.

Application Number Filing DatePatented/Pending/Abandoned

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**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION**

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**Docket No. 42141/RJP/E264**

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**POWER OF ATTORNEY:** I hereby appoint the following attorneys and agents of the law firm CHRISTIE, PARKER & HALE, LLP to prosecute this application and any international application under the Patent Cooperation Treaty based on it and to transact all business in the U.S. Patent and Trademark Office connected with either of them in accordance with instructions from the assignee of the entire interest in this application; or from the first or sole inventor named below in the event the application is not assigned; or from \_\_ in the event the power granted herein is for an application filed on behalf of a foreign attorney or agent.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**DECLARATION AND POWER OF ATTORNEY  
FOR PATENT APPLICATION**

**Docket No. 42141/RJP/E264**

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